TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES

NOTE: The symbol (*) denotes that a word, number, phrase, sentence or specification has been changed, deleted or added to the previous TEES Document.

NOVEMBER 19, 1999

STATE OF CALIFORNIA
DEPARTMENT OF TRANSPORTATION

GRAY DAVIS
Governor

MARIA CONTRERAS-SWEET
Secretary
Business, Transportation & Housing Agency

JOSE MEDINA
Director
Department of Transportation

RANDELL H. IWASAKI
Deputy Director
Maintenance and Operations

KIM NYSTROM
Program Manager (Acting)
Traffic Operations

SOMPOL CHATUSRIPITAK
Chief, ITS Development and Support

TABLE OF CONTENTS

CHAPTER 1

GENERAL SPECIFICATIONS FOR ELECTRICAL EQUIPMENT

TABLE OF CONTENTS

CHAPTER 1 SECTION 1

GLOSSARY

1.1 Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:

A	**-**	**Ampere**
AC	**-**	**Alternating Current**
AC+	**-**	**120 Volts AC, 60 hertz ungrounded power source**
AC-	**-**	**120 Volts AC, 60 hertz grounded return to the power source**
AGENCY	**-**	**Purchasing Government Agency**
ANSI	**-**	**American National Standard Institute**
ASCII	**-**	**American Standard Code for Information Interchange**
Assembly	**-**	**A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules**
ASTM	**-**	**American Society for Testing and Materials**
AWG	**-**	**American Wire Gage**
C	**-**	**Celsius**
C Language	**-**	**The ANSI C Programming Language**
Cabinet	**-**	**An outdoor enclosure generally housing the controller unit and associated equipment**
Certificate of Compliance	**-**	**A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications**
Channel	**-**	**An information path from a discrete input to a discrete output**
CIA	**-**	**CMS Controller Isolation Assembly**
CIP	**-**	**CMS Interface Panel**

CMOS	**-**	**Complementary Metal Oxide Semiconductor**
CMS	**-**	**Changeable Message Sign**
CMS SYSTEM	**-**	**Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to operate the system.**
Component	**-**	**Any electrical or electronic device**
Contractor	**-**	**The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party(s) of the second part or legal representative**
Controller Unit	**-**	**That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly**
CPDA	**-**	**CMS Pixel Driver Assembly**
CPDM	**-**	**CMS Pixel Driver Module**
CPMM	**-**	**CMS Pixel Matrix Module**
CPU	**-**	**Central Processing Unit**
CR	**-**	**ACIA Control Register**
CRC	**-**	**Cyclic Redundancy Check**
DAT Program	**-**	**The AGENCYs Diagnostic and Acceptance Test Program**
dB	**-**	**Decibel**
dBa	**-**	**Decibels above reference noise, adjusted**
DC	**-**	**Direct Current**
DIN	**-**	**Deutsche Industrie Norm**
DMA	**-**	**Direct Memory Access**
DTA	**-**	**Down Time Accumulator**
EG	**-**	**Equipment Ground**

EIA	**-**	**Electronic Industries Association**
EMI	**-**	**Electro Magnetic Interference**
Engineer	**-**	**The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them**
EPROM	**-**	**Ultraviolet Erasable, Programmable, Read Only Memory Device**
EEPROM	**-**	**Electrically Erasable, Programmable, Read Only Memory Device**
Equal	**-**	**Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device**
ETL	**-**	**Electrical Testing Laboratories, Inc.**
Firmware	**-**	**A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM**
FLASH	**-**	**A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features**
FPA	**-**	**Front Panel Assembly**
HEX	**-**	**Hexadecimal**
Hz	**-**	**Hertz**
IC	**-**	**Integrated Circuit**
I.D.	**-**	**Identification**
IEEE	**-**	**Institute of Electrical and Electronics Engineers**
ISO	**-**	**International Standards Organization**
Jumper	**-**	**A means of connecting/disconnecting two or more conductive by soldering/desoldering a conductive wire or by PCB post jumper**
KB	**-**	**Kilobytes**

Laboratory	**-**	**The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract**
LED	**-**	**Light Emitting Diode**
LOGIC	**-**	**Negative Logic Convention (Ground True) State**
LSB	**-**	**Least Significant Byte**
lsb	**-**	**Least Significant Bit**
MB	**-**	**MegaByte**
MSB	**-**	**Most Significant Byte**
msb	**-**	**Most Significant Bit**
m	**-**	**Milli**
MCU/MPU/ IMP	**-**	**Micro Controller Unit, Microprocessor Unit, or Integrated Multiprotocol Processor**
MIL	**-**	**Military Specifications**
MODEM	**-**	**Modulation/Demodulation Unit**
Module	**-**	**A functional unit that plugs into an assembly**
Motherboard	**-**	**A printed circuit connector interface board with no active or passive components**
MOS	**-**	**Metal-Oxide Semiconductor**
MOV	**-**	**Metal-Oxide Varistor**
MS	**-**	**Military Standards**
M/170	**-**	**Program Module/Model 170 Controller Unit Connector**
M/170E	**-**	**Model 170E Auxiliary Board Connector**
N	**-**	**Newton: SI unit of force**
N.C.	**-**	**Normally closed contact**
N.O.	**-**	**Normally open contact**

NA	**-**	**Presently Not Assigned. Cannot be used by the contractor for other purposes**
NEMA	**-**	**National Electrical Manufacturer's Association**
NETA	**-**	**National Electrical Testing Association, Inc.**
n	**-**	**nano**
NLSB	**-**	**Next Least Significant Byte**
nlsb	**-**	**Next Least Significant Bit**
NMSB	**-**	**Next Most Significant Byte**
nmsb	**-**	**Next Most Significant Bit**
PCB	**-**	**Printed Circuit Board**
PDA	**-**	**Power Distribution Assembly**
PLA/PAL	**-**	**Programmable Array Logic Device**
Power Failure	**-**	**A Power Failure is said to have occurred when the incoming line voltage falls below 92 +/- 2 VAC for 50 ms. See Power Conditions.**
Power Restoration	**-**	**Power is said to be restored when the incoming line voltage equals or exceeds 97 +/- 2 VAC for 50 ms. See Power Conditions.**
Power Conditions	**-**	**16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (67 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.**
ppm	**-**	**Parts per million**
PWM	**-**	**Pulse Width Modulation**
RAM	**-**	**Random Access Memory**
RDR	**-**	**ACIA Receiver Data Register**
RF	**-**	**Radio Frequency**

RMS	**-**	**Root-Mean-Square**
ROM	**-**	**Read Only Memory Device**
RTC	**-**	**Model 170E Controller Unit Real Time Clock. This circuitry provides a 170E CPU IRQ Interrupt pulse clocked off of the local power company's line frequency every 16.67 ms.**
RTCA	**-**	**Real Time Clock Adjuster Circuitry**
RTS	**-**	**Request to Send**
R/W	**-**	**Model 170E Controller Unit Read/Write Control Line**
SCI	**-**	**Serial Communications Interface**
SDLC	**-**	**Synchronous Data Link Control**
S	**-**	**Logic State**
s	**-**	**second**
Second Sourced	**-**	**Produced by more than one manufacturer**
SR	**-**	**ACIA Status Register**
SRAM	**-**	**Static Random Access Memory Device**
SW	**-**	**Switch**
TB	**-**	**Terminal Block**
TDR	**-**	**ACIA Transmit Data Register**
TOD	**-**	**Time Of Day Clock**
Triac	**-**	**Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit**
TTL	**-**	**Transistor-Transistor Logic**
Thumb Screw Device	**-**	**(TSD) A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No.2 shall be flat black.)** **TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal.**

TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal.
TSD No.3 - M3 SOUTHCO #47-82-101-10 or equal.

µ	**-**	**Micro**
UL	**-**	**Underwriter's Laboratories, Inc.**
VAC	**-**	**Voltage Alternating Current**
VDC	**-**	**Voltage Direct Current**
VMA	**-**	**Valid Memory Address**
VME	**-**	**Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2**
x	**-**	**Number Value**
XX	**-**	**Manufacturer's Option**
WDT	**-**	**Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts**

CHAPTER 1 SECTION 2

GENERAL

1.2.1
In CASE of CONFLICT, the individual chapter shall govern over Chapter 1.

1.2.2
All furnished equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

1.2.3
INTERCHANGEABILITY - The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES	ASSOCIATED DEVICES
Output File #1 & #2	- Model 200 Switch Pack - Model 210 Monitor Unit - Model 430 Heavy Duty Relay
Input File	- Models 222, 224, & 232E Detectors - Models 242 & 252 Isolators
PDA #2	- Model 204 Flasher Unit - Model 206 Power Supply Module
PDA #3	- Model 200 Switch Pack - Model 206 Power Supply Module - Model 208 Monitor Unit - Model 430 Heavy Duty Relay
PDA #4	- Model 206 Power Supply - CMS Isolation Module
Model 170E Controller Unit	- Cabinet Models 332, 334 & 336 - Model 400 MODEM - Model 412C Program Module
Model 2070 Controller Unit	- Cabinet Models 332, 334,, 336 & ITS - Model 2070-1 CPU Module - Model 2070-2 Field I/O Module - Model 2070-3 Front Panel Assembly - Model 2070-4 Power Supply - Model 2070-5 VME Cage Assembly

	- Model 2070-6 Serial Comm Module
	- Model 2070-7 Serial Comm Module
Model 2070N Controller Unit	- Model 2070 Controller Unit
	- Model 2070-8 NEMA Module
	- Model 2070-2B Field I/O Module
Pixel Driver Assembly	- Pixel Driver Module

1.2.4 DOCUMENTATION

1.2.4.1

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 215.9 mm by 279.4 mm paper, with the exception that schematics, layouts, parts lists and plan details may be on 279.4 mm by 431.8 mm sheets, with each sheet neatly folded to 215.9 mm by 279.4 mm size. Manual text font shall be HELVETICA BOLD. Text characters shall be no more than 10 characters per 25.4 mm and 7 lines per 25.4 mm, with the exception of schematic text, which shall be no more than 18 characters per 25.4 mm and 11 lines per 25.4 mm.

1.2.4.2

Each manual shall include the following parts in the order listed:

1. **Table of Contents**
2. **Glossary**
3. **General Description**
4. **General Characteristics**
5. **Installation**
6. **Adjustments**
7. **Theory of Operation**
    a. **Systems Description (include block diagram).**
    b. **Detailed Description of Circuit Operation.**
8. **Maintenance**
    a. **Preventive Maintenance.**
    b. **Trouble Analysis.**
    c. **Trouble Shooting Sequence Chart.**
    d. **Wave Forms.**
    e. **Voltage Measurements.**
    f. **Alignment Procedures.**
9. **Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).**
10. **Electrical Interconnection Details & Drawings.**

11. **Schematic and Logic Diagram.**
12. **Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.**
13. **The date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals.**

1.2.4.3
Manuals for the cabinet shall be furnished in the cabinet plastic pouch.

1.2.4.4
A preliminary draft of the manual shall be submitted to the Engineer for approval prior to final printing.

1.2.5
PACKAGING - Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the styrofoam.

1.2.6
DELIVERY - Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.2.7 METALS

1.2.7.1
ALUMINUM - Sheet shall be 3.175 mm (0.125-inch) minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.2.7.2
STAINLESS STEEL - Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.2.7.3
COLD ROLLED STEEL - Sheet, Rod, Bar and Extruded shall be Type 1018/1020.

1.2.7.3.1
Plating - All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

1.2.7.4
All sharp edges and corners shall be rounded.

1.2.8

All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

1.2.9

Within the circuit of any device, module, or PCB, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded conductor. They shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.

CHAPTER 1 SECTION 3

COMPONENTS

1.3.1
GENERAL - All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

1.3.1.1
When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

1.3.1.2
The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.3.2 ELECTRONIC COMPONENTS

1.3.2.1
No device shall be socket mounted unless specifically called out.

1.3.2.2
No component shall be operated above 80% of its maximum rated voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

1.3.2.3
No component shall be provided where the manufactured date is 2 years older than the contract award date. The design life of all components, operating for 24 hours a day and operating in their circuit application, shall be 10 years or longer.

1.3.2.4
Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid- state switches, optical isolators and transistor arrays. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

1.3.2.5
The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.3.3
CAPACITORS - The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements shall be resistant to cracking, peeling and discoloration. All capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

1.3.4
POTENTIOMETERS - Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Under 1 Watt potentiometers shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.5
RESISTORS - Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors shall be insulated and shall be marked with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -37 ^{0}C and 74 ^{0}C.

1.3.5.1
Special ventilation or heat sinking shall be provided for all 2- watt or greater resistors. They shall be insulated from the PCB.

1.3.6 SEMICONDUCTOR DEVICES

1.3.6.1
All solid-state devices, except LED's, shall be of the silicon type.

1.3.6.2
All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.

1.3.6.3
All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.3.6.4
Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.

1.3.7
TRANSFORMERS AND INDUCTORS - All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be

protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.3.8
TRIACS - Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with a machine screw and nut with integral lockwasher.

1.3.9 CIRCUIT BREAKERs shall be listed by UL or ETL. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from -18 degrees C to 50 degrees C. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal).

1.3.10
All FUSEs shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the holder. Fuses shall be easily accessible and removable without use of tools.

1.3.11 SWITCHES

1.3.11.1
DIP - Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 ma, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 ma, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal).

1.3.11.2
LOGIC - The switch contacts shall be rated for a minimum of one ampere resistive load at 120 VAC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.3
CONTROL - The switch contacts shall be rated for a minimum of five ampere resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.4
POWER - Ratings shall be the same as CONTROL, except the contact rating shall be a minimum of ten amperes at 125 VAC.

1.3.12

TERMINAL BLOCKS - The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum. The terminal screws shall be 7.938 mm minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.3.13

WIRING, CABLING AND HARNESSES

1.3.13.1

HARNESSES shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize crosstalk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements.

1.3.13.2

Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.3.13.3

Wiring shall be routed to prevent conductors from being in contact with metal edges. Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.3.13.4

All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.3.13.5

Conductor color identification shall be as follows:

Grounded AC circuits - gray or white
Equip. Ground - solid green or continuous green color with 1 or more yellow stripes.
DC logic ground - continuous white with a red stripe.
Ungrounded AC+ - continuous black or black with colored stripe.
DC logic ungrounded or signal - any color not specified

1.3.14

INDICATORS AND CHARACTER DISPLAYS - All indicators and character displays shall be readily visible at a radius of up to 1.2 m (4 feet) within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

1.3.14.1
INDICATORS - All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and red when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for Models 208, 210, 212, 222, 232, 242 and 252, as well as a clearance of 30 degrees minimum for Models 200, 204 and 206.

1.3.14.2
CHARACTER DISPLAYS - Liquid Crystal Displays (LCD) shall operate at temperatures of -20 ^{0}C to +70 ^{0}C.

1.3.15 CONNECTORS

1.3.15.1
GENERAL - All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1.3.15.2
The TYPE T connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 6.35 mm or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.15.3
PLASTIC CIRCULAR and M TYPE CONNECTORS - Pin and socket contacts for connectors shall be beryllium copper construction subplated with 0.00127 mm nickel and plated with 0.00076 mm gold. Pin diameter shall be 1.57 mm. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.15.4
CARD EDGE and TWO-PIECE PCB CONNECTORS

1.3.15.4.1
PCB edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	**600 VAC (RMS)**
Current Rating:	**5.0 amperes**
Insulation Material:	**Diallyl Phthalate or Thermoplastic**
Insulation Resistance:	**5,000 megohms**
Contact Material:	**Copper alloy plated with 0.00127 mm (0.00005 inch) of nickel and 0.000381 mm (0.000015 inch) of gold**

Contact Resistance: 0.006 ohm maximum

1.3.15.4.2
The two-piece PCB connector shall meet or exceed the DIN 41612.

1.3.15.4.3
The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 3.96 mm (0.156 inch) contact centers.

1.3.15.4.4
The PCB 28/56 Connector shall have 28 independent contacts per side, dual sided with 3.96 mm (0.156 inch) contact centers.

1.3.15.4.5
The PCB 36/72 Connector shall have 36 independent contacts per side, dual sided with 2.54 mm (0.100 inch) contact centers.

1.3.15.4.6
The PCB 43/86 Connector shall have 43 independent contacts per side, dual sided with 2.54 mm (0.100 inch) contact centers.

1.3.15.5
WIRE TERMINAL CONNECTORS - Each wire terminal shall be solderless with PVC insulation and a heavy duty short -locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

1.3.15.6
FLAT CABLE CONNECTORS - Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 508 nm of gold over 1270 nm of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 megohms minimum.

1.3.15.7
PCB HEADER POST CONNECTORS - Each PCB header post shall be 1.0 mm square by 8.7 mm high; shall be mounted on 4.0 mm centers; and shall be tempered hard brass plated with 381 nm of gold over 1.270 mm of nickel.

1.3.15.8
PCB HEADER SOCKET CONNECTORS - Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 562 nm of gold over 1270 nm of nickel.

1.3.16
SURGE PROTECTION DEVICE - A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5

of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 amperes. It shall have the following ratings:

IMPULSE BREAKDOWN:	**Less than 1,000 volts in less than 0.1 us at 10 KV/us.**
STANDBY CURRENT:	**Less than 1 ma.**
STRIKING VOLTAGE:	**Greater than 212 volts.**

CHAPTER 1 SECTION 4

MECHANICAL

1.4.1
ASSEMBLIES - All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 19.05 mm from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.2
PCB DESIGN - No components, traces, brackets or obstructions shall be within 3.175 mm of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.4.3
MODEL NUMBERS - The manufacturer's model number, serial number, and circuit issue or revision number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the State model number shall be displayed on the front panel in bold type, at least 6.35 mm high.

1.4.4
All PCB connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

1.4.5
All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.4.6
WORKMANSHIP - Workmanship shall conform with the requirements of this specification and be in accordance with the highest industry standards.

1.4.7
TOLERANCES - The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	**+/-**	**1.334 mm (0.0525 inch)**
PCB	**+/-**	**0.254 mm (0.010 inch)**
Edge Guides	**+/-**	**0.381 mm (0.015 inch)**

CHAPTER 1 SECTION 5

ENGINEERING

1.5.1 HUMAN ENGINEERING

1.5.1.1
The equipment shall be engineered for simplicity, ease of operation and maintenance.

1.5.1.2
Knobs shall be a minimum of 12.7 mm in diameter and a minimum separation of 12.7 mm edge to edge.

1.5.1.3
PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 22.24 N or greater than 222.4 N for insertion or removal.

1.5.2
DESIGN ENGINEERING - The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. Personnel shall be protected from all dangerous voltages.

1.5.3
GENERATED NOISE - No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.

CHAPTER 1 SECTION 6

PRINTED CIRCUIT BOARDS

1.6.1 DESIGN, FABRICATION AND MOUNTING

1.6.1.1
All contacts on PCBs shall be plated with a minimum thickness of 0.000763 mm gold over a minimum thickness of 0.001905 mm nickel.

1.6.1.2
PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

1.6.1.3
Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:

1.6.1.3.1
NEMA FR-4 glass cloth base epoxy resin copper clad laminates 1.590 mm minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 0.556 kilogram per square meter with adequate cross section for current to be carried. All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

1.6.1.3.2
In Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better. Class of permissible bow or twist shall be Class C (Table V) or better. Class of permissible warp or twist shall be Class A (Table II) or better.

1.6.1.3.3
Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.

1.6.1.4
The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:

1.6.1.4.1
Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 10 degrees C or more shall be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.

1.6.1.4.2
When completed, all residual flux shall be removed from the PCB.

1.6.1.4.3
The resistance between any 2 isolated, independent conductor paths shall be at least 100 megohms when a 500 VDC potential is applied.

1.6.1.4.4
All PCBs shall be coated with a moisture resistant coating.

1.6.1.4.5
Where less than 6.35 mm lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.79375 +/-0.39624 mm thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

1.6.1.5
Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 1.143 +/- 0.127 mm for 2.54 mm spacing and 1.40 +/- 0.127 mm for 3.96 mm spacing.

1.6.2 SOLDERING

1.6.2.1
Hand soldering shall comply with Military Specification MIL-STD-2000.

1.6.2.2
Automatic flow soldering shall be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within +/- 8 degrees C of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.6.2.2.3
If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

1.6.3
DEFINITIONS - Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.

CHAPTER 1 SECTION 7

QUALITY CONTROL

1.7.1
COMPONENTS - All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

1.7.2
SUBASSEMBLY, UNIT OR MODULE - Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.7.3
PREDELIVERY REPAIR

1.7.3.1
Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.7.3.2
PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

1.7.3.3
Hand soldering is allowed for printed circuit repair.

CHAPTER 1 SECTION 8

ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

1.8.1
GENERAL - The requirements called out in these specification dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

1.8.2
CERTIFICATION - These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with these specifications.

1.8.3
INSPECTION - A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

1.8.4
ENVIRONMENTAL & ELECTRICAL - All components shall properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note "Power Failure / Restoration" limits
Frequency: 60 (+/-3.0) Hertz
Humidity: 5% to 95%
Ambient Temperature: -37 ^{0}C to +74 ^{0}C
Shock - Test per Specification MIL-STD-810E Method 516.4.
Vibration - per Specification MIL-STD-810E Method 514.4, equipment class G.

1.8.4.1
All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

1.8.4.2
All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a State accepted cabinet connected to the commercial power lines.

1.8.4.3
The power line surge protection shall enable the equipment being tested to withstand (nondestructive) and operate normally following the discharge of a 25 microfarad capacitor, charged to plus and minus 2,000 volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 20 ^{0}C (+/-5) ^{0}C and at 120 (+/-12) VAC.

1.8.4.4
The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 20 ^{0}C (+/-5) ^{0}C and at 120 (+/-12) VAC.

1.8.4.5
The controller unit communications modules shall be tested resident in a State-accepted controller unit which in turn is housed in the cabinet.

1.8.4.6
CMS system equipment will be tested for compliance as a complete system with power from commercial power lines applied at the CMS CIP Panel and the CMS Power Surge Protector deactivated or removed.

1.8.4.7
Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

1.8.4.8
All equipment shall continue normal operation when subjected to the following:

1.8.4.8.1
Low Temperature Test - With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be lowered from 20 ^{0}C to –37 ^{0}C at a rate of not more than 18 ^{0}C per hour. The item shall be cycled at -37 ^{0}C for a minimum of 5 hours and then returned to 20 ^{0}C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.2
High Temperature Test - With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be raised from 20 ^{0}C to 70 ^{0}C at a rate of not more than 18 ^{0}C per hour. The item shall be cycled at 70 ^{0}C for 5 hours and then returned to 20 ^{0}C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.3
All equipment shall resume normal operation following a period of at least 5 hours at -37 ^{0}C and less than 10 percent humidity and at least 5 hours at 70 ^{0}C and 22% humidity, when 90 VAC is applied to the incoming AC.

1.8.4.9
The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY
AT BAROMETRIC PRESSURES (29.92 In. Hg.)

Ambient Temperature/ Dry Bulb (in ^{0}C)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in ^{0}C)
-37.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
74.0	18	42.7

1.8.4.10
All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.8.5
CONTRACTOR'S TESTING CERTIFICATION

1.8.5.1
A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.8.5.2
The quality control procedure and test report format shall be sullied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all items.

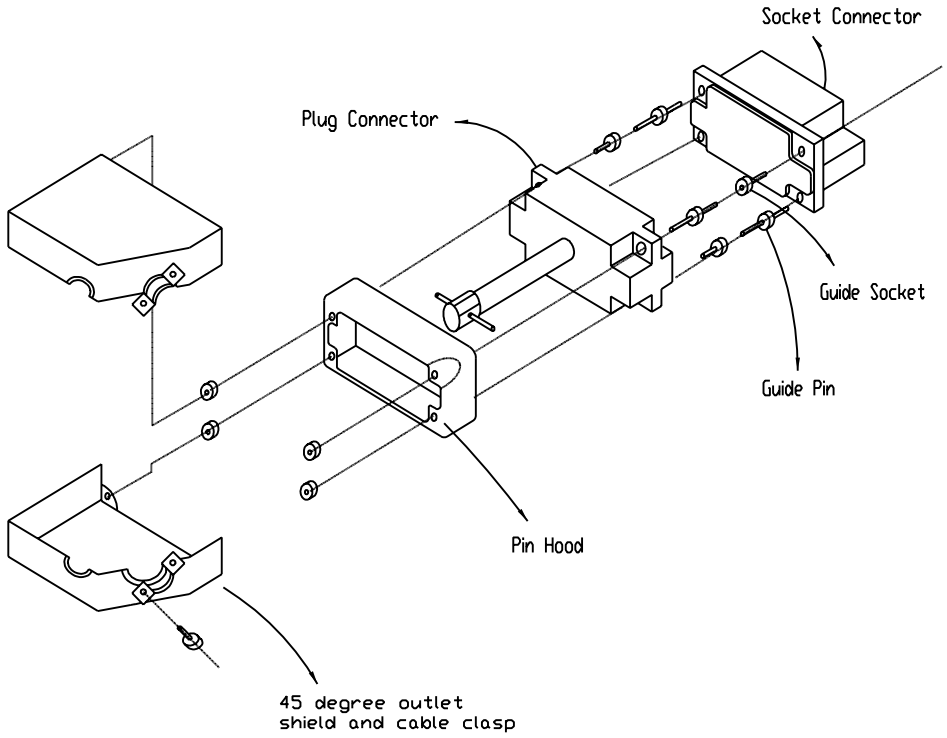
SECTION 9

CHAPTER DETAILS

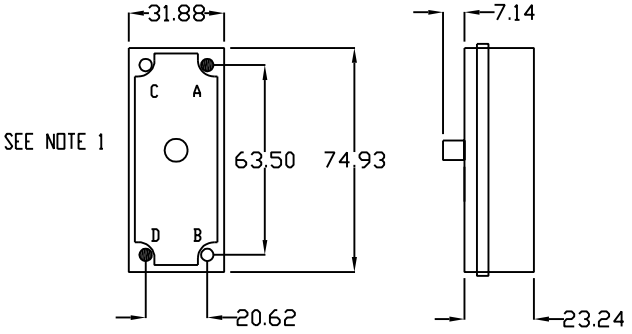
TABLE OF CONTENTS

Section Notes:

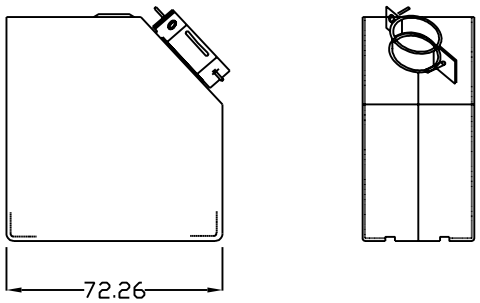
1. **All dimensions are in millimeters.**
2. **M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 megohms. The contacts shall be secured in the blocks with stainless steel springs.**
3. **M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.**
4. **Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.**



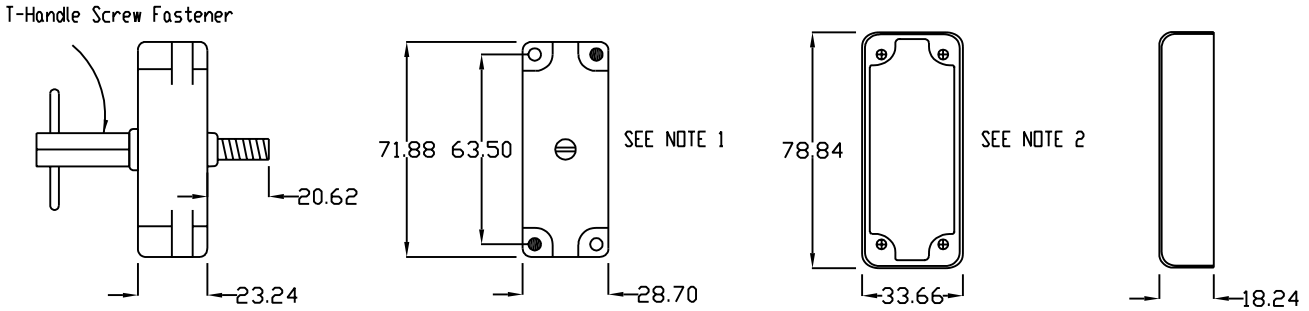
M104 CONNECTOR C1 DETAIL



M104 SOCKET CONNECTOR



M104 SHIELD



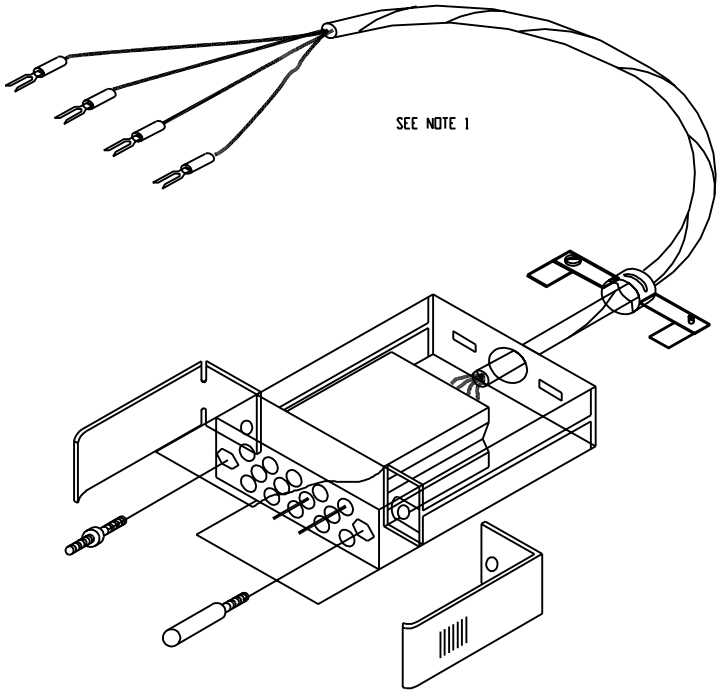
CONNECTOR C1P

M104 HOOD

NOTES:

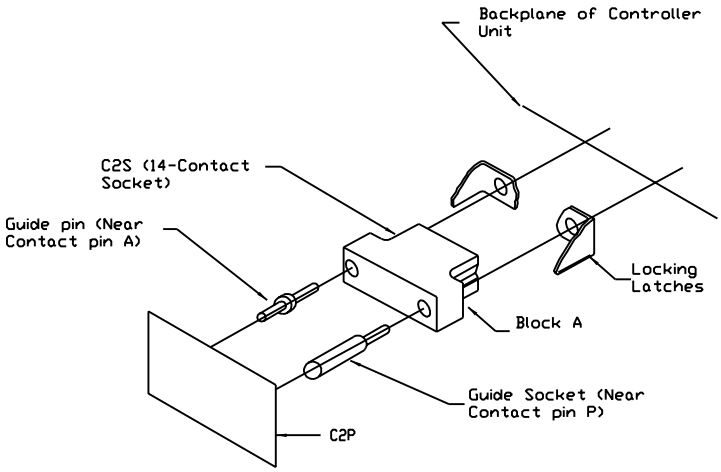
1. The darker circles denote guide pin location and the open circles are guide sockets.
2. Provide clearance for M104 plug with hood when mounting to it's socket.

	TITLE: CONNECTOR DETAIL - M104	
	NO SCALE	
	TEES, NOV 19, 1999	1-9-1

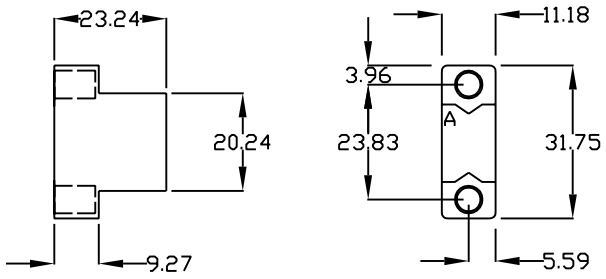


C2P MODEM INTERCONNECT HARNESS

C2P CONNECTOR ASSIGNMENT		
PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	BLACK
C	AUDIO OUT	RED
E	AUDIO OUT	GREEN



CONNECTOR C2 DETAIL

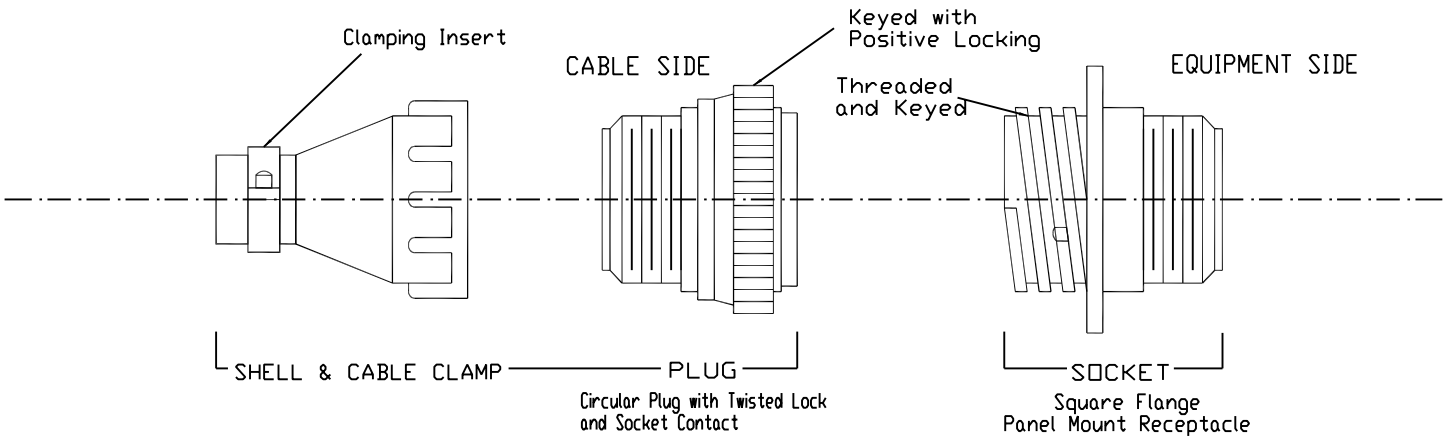


CONNECTOR C2S

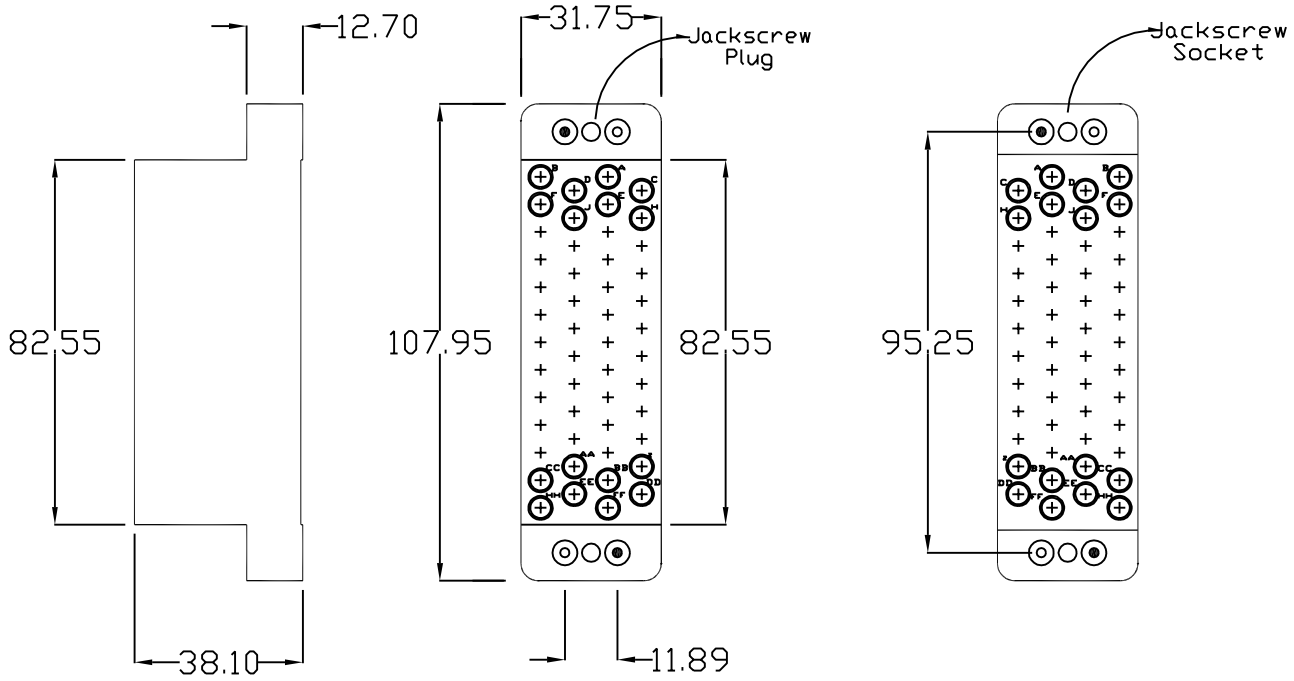
NOTES:

1. Cable length shall be 914 mm minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.

TITLE: CONNECTOR DETAIL - M14	
NO SCALE	
TEES, NOV 19, 1999	1-9-2



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR



CONNECTOR PIN ARRANGEMENT

NOTES:

1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.

2. Key: o - socket
   ● - plug

	TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTORS	
	NO SCALE	
	TEES, NOV 19, 1999	1-9-3

CHAPTER 2

SPECIFICATIONS FOR MODEL 170E ENHANCED CONTROLLER UNIT AND ASSOCIATED MODULES

TABLE OF CONTENTS

CHAPTER 2 SECTION 1

GENERAL

2.1.1
System READ Access Time - With Model 412C Module Resident in the Controller Unit, valid data shall be present at the MPU at least 100 ns prior to the end of the machine cycle.

2.1.2
DIAGNOSTIC AND ACCEPTANCE TEST (DAT) PROGRAMS - The DAT-170E Program shall be provided resident on the Model 412C Program Module U1 memory device and on the CPU U6 memory device. A copy of the DAT Programs will be available to the contractor at no charge.

2.1.3
If a PAL, EPROM, or ROM device is used in address decoding and timing algorithms, the device code listing together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.

2.1.4
SYSTEM ADDRESS ORGANIZATION - The system address organization of the Model 170E shall consist of two addressing configurations. The Decoder Input shall be furnished jumpered in address configuration 1. The internal module address organization shall be as specified in the appropriate module section.

2.1.4.1
The two addressing configurations shall be selectable by use of one post jumper. The jumper shall control the Logic State of one Decoder Circuit Input. The logic line shall be a three-post type with the two logic levels on the outer posts. The following input line state conditions shall cause the Decoder circuit to provide the associated address configurations:

CONFIGURATION	LINE	FUNCTION
1	+5 VDC	170E / 412C
2	DC GND	170E INTERNAL / 170

2.1.4.2
CONFIGURATION 1 Address Organization

FUNCTION	ADDRESS RANGE		COMMENTS	
CPU SRAM	0000	-	0FFF	
U4 Memory	1000	-	3FFF	412C
Reserved	4000	-	4FFF	
DTA Minutes	5000		READ	
DTA Reset	5000		WRITE	
INPUT / OUTPUT	5001	-	5008	
	5009	-	500A WRITE	
RESTART State	5004		BIT 1 READ	
DTA Seconds	500F		READ	
Reserve	5009	-	500E READ	
	500B	-	500F WRITE	

	5010 - 5FFE		
CPU STATUS	5FFF	READ	Bit 1 - ACIA #1 IRQ Bit 2 - ACIA #2 IRQ Bit 3 - ACIA #3 IRQ Bit 4 - ACIA #4 IRQ Bit 5 - Reserved Bit 6 – Address Configuration Bit 7 - DTA Timeout Bit 8 - RTC IRQ
RTC Reset	5FFF	WRITE	
ACIA #1	6000	WRITE CR, READ SR	
ACIA #1	6001	WRITE TDR, READ RDR	
ACIA #2	6002	WRITE CR, READ SR	
ACIA #2	6003	WRITE TDR, READ RDR	
ACIA #3	6004	WRITE CR, READ SR	
ACIA #3	6005	WRITE TDR, READ RDR	
ACIA #4	6006	WRITE CR, READ SR	
ACIA #4`	6007	WRITE TDR, READ RDR	
Reserve	6008 - 600F		
CPU SRAM	6010 - 6FFF		

PROGRAM MODULE-

Memory Write Protect	7000 WRITE
I.D. Feature	7000 READ
I.D. Location	7001 READ
	7001 WRITE Reserve
Reserve	7002 - 7009
	700B - 700E WRITE
	700F READ
RTCA Valid/Reset	700A
RTCA Counters 1 to 4	700B - 700E READ
U3 Memory	7010 - 7FFF
U1 & U2 Memory	8000 - FFFF

Note -- Address locations noted as "Reserve" are assignable by the Agency only and shall not be used. CPU STATUS Bit 6: "0" equals Address Configuration 1 and "1" equals Address Configuration 2.

2.1.4.3
CONFIGURATION 2 Address Organization - This configuration provides all Model 412C Program Module features internal to the controller unit. The address organization is the same as CONFIGURATION 1 with the following exceptions:

CPU SRAM	0000 - 3FFF	U3 & U4 Memory internal
	6010 - 6FFF	
	7010 - 7FFF	
U6 EPROM	8000 - FFFF	U1 & U2 Memory internal

2.1.5
Each memory device shall stabilize to normal operation within 10 ms following Power Restoration and shall be in Standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

MEMORY	ACTIVE	STANDBY	POWERDOWN
EPROM	100 ma	40 ma	-
SRAM	85 ma	20 ma	100 ua (non-internal power)

2.1.6
CPU EPROM MEMORY SOCKETS shall be a 28 Pin AMP Diplomate LF #641894-2, or equal. The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC or equal. Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "... or equal MPU" Pin / Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.

CHAPTER 2 SECTION 2

MODEL 170E CONTROLLER UNIT

2.2.1 UNIT COMPOSITION

2.2.1.1
The Model 170E Controller Unit shall consist of the following:

- **Central Processing Unit (CPU)**
- **Input / Output Interface**
- **Unit Chassis**
- **M170E Auxiliary Board**
- **Model 412C Program Module**
- **Unit Power Supply with external power connection**
- **Unit Standby Power**
- **Front Panel Assembly**
- **Internal System Interface**
- **Connectors C1S, C2S, C20S, C30S, C40S, and T-1**
- **Communications System Interface**

2.2.1.2
The 170E shall be delivered pinned for Configuration 1 Addressing.

2.2.1.3
The composition weight shall not exceed 25 pounds.

2.2.2
CENTRAL PROCESSING UNIT (CPU)

2.2.2.1
The CPU shall be provided with an MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1
Non-Maskable Interrupt (NMI) - The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2
Reset Interrupt (RES) - The RES is exclusively assigned to Power Restoration and MPU Startup. The RES line shall go LOW 3 (±1) ms following the NMI going LOW. The line shall remain LOW until 150 (±75) ms after Power Restoration.

2.2.2.1.3
Interrupt Request (IRQ) - The IRQ Line shall be jointly used by the RTC and Four ACIAs to initiate IRQ to the MPU.

2.2.2.1.3.1
Real Time Clock (RTC) - Real Time Clock circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270 degree to 330 degree portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at Bit 8, Address 5FFF (STATUS) and reset by a WRITE to Address 5FFF.

2.2.2.1.3.2
ACIA - Four ACIAs shall be provided, each capable of receiving and transmitting up to eight-bits of parallel data from the MPU for serial data communications. The ACIA shall have 4 registers which are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing in the Transmit Data Register (TDR) and in the Control Register (CR).

2.2.2.1.3.3
Each ACIA shall be provided with a 2 post type jumper between its IRQ output and the MPU IRQ input. The 170E shall be delivered with these jumpers installed.

2.2.2.2
CPU Clock Timing - The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 (±0.0015) us. The machine cycle time selection shall be by Post Jumper (Three Post Type) with jumper in for 1.302 us. The CPU clock circuitry shall be located no further than 50.80 mm from the MPU clock pin inputs.

2.2.2.3
SRAM Memory, DALLAS 1235Y or equal, shall be provided.

2.2.2.4
AN EPROM Memory, INTEL 24256A or equal, shall be provided in socket U6.

2.2.2.5
Restart Timer – A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (±0.25) seconds, its output state shall go to LOW and remain in that state for 50 (±24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to "0".

2.2.3
DOWNTIME ACCUMULATOR (DTA)

2.2.3.1
A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following Power Restoration.

2.2.3.2
The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ±1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall reset to 0 by a WRITE to Address 5000. The DTA shall READ Minutes at Address 5000 and Seconds at Address 500F. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and reset the other register to "0".

2.2.4
TOTAL CURRENT DRAIN FOR DTA AND RESTART TIMER CIRCUITRY (powerdown mode) shall not exceed 400 ua at 5 VDC, 35^0C while timing and 100 ua at 5 VDC when timeout is latches.

2.2.5
INPUT / OUTPUT INTERFACE

2.2.5.1
Input / Output Interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of the MPU read / write command at the time the given address is valid.

2.2.5.2
Output Interface - The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.5.3
Input Interface - The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC, shall be turned OFF (false) when the input current is less than 100 ua or the input voltage exceeds 8.5 VDC, shall pull up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.6
UNIT CHASIS - The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 19 inch rack. The enclosure shall be designed for convenient removal of PCBs without the use of tools.

2.2.7 UNIT POWER SUPPLY

2.2.7.1
A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1. 1000 mA at +12 VDC
2. 300 mA at -12 VDC
3. 500 mA at + 5 VDC
4. 400 mA at - 5 VDC

2.2.7.2
The DC ground shall not be connected to equipment ground.

2.2.7.3
Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ±17 ms beyond the NMI line going LOW.

2.2.7.4
The maximum DC voltage generated shall not exceed 45 volts.

2.2.7.5
The Power Supply shall be so designed that no further filtering regulation is needed for the required DC voltages.

2.2.7.6
Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be COR COM 3VS1 or equal.

2.2.8 UNIT STANDBY POWER

2.2.8.1
A standby power supply shall be provided to retain power (minimum of 72 hrs) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup Capacitors, capacitor charging circuitry and power sense / transfer circuitry.

2.2.8.2
The power sense / transfer circuitry shall sense power loss and transfer battery power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.

2.2.8.3
A charging circuit which shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.

2.2.9 FRONT PANEL ASSEMBLY

2.2.9.1
The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.2.9.2
The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to equipment ground through Connector C3.

2.2.9.3
The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 10.16 mm high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.2.9.4
The front panel shall be provided with 10 LED CALL / ACTIVE indicators.

2.2.9.5
A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 48.39 mm^2 and shall be mounted on a minimum of 12.7 mm centers; shall have an actuation force between 50 and 100 grams and shall provide a positive tactical indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.

2.2.9.6
The front panel shall be provided with a toggle LOGIC switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.2.9.7
An ON-OFF toggle CONTROL switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 amperes, dependent upon the controller unit power requirements.

2.2.9.8
The front panel, under the legend "OPERATING INSTRUCTIONS", shall include a framework to retain a card, 101.60 mm wide by 152.40 mm high by 1.59 mm thick.

2.2.10 INTERNAL SYSTEM INTERFACE

2.2.10.1
PCB to PCB Connector spacing shall be a minimum of 25.4 mm. Continuous nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.

2.2.10.2
Two PCB 22/44S Connectors shall be provided for the MODEM Modules MC1 and MC2, and two PCB 36/72S Connectors shall be provided for the M170 Connector / Program Module and the M170 Connector / M170E Auxiliary Board.

2.2.10.3
The depth placement of the vertical M/170 Connector shall be such that the Program Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

2.2.11 DATA AND ADDRESS BUS REQUIREMENTS

2.2.11.1
All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 ns.

2.2.11.2
All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

2.2.12 CONNECTOR REQUIREMENTS

2.2.12.1
Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.

2.2.12.2
The Model 400 MODEM and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12.3
ACIA 4 RS 232 Signal Lines and Buffered mirrored signals NMI, RES and ROT Shall be internally route to M170 and M170E as noted in Pin Assignments under Section 5 Details.

2.2.13 COMMUNICATION SYSTEM INTERFACE

2.2.13.1
The communication system shall consist of the CPU, ACIAs, motherboard connectors and lines, MODEM Module Connectors MC1 & MC2 and interfaces between ACIA & MODEM and both MODEM and ACIA to C2S, C20S, C30S, C40S and Connector / T-1 Terminal. The interface between the ACIA and MODEM shall comply with EIA RS-232-C Standards and all functions under T-1, C2, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the MODEM. The RTS and TX Data lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.2.13.2
C20S, C30S, and C40S Connectors shall meet the requirements for the C2S Connector.

2.2.13.3
A minimum of four baud rate frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz and 153.6 kHz shall be provided at the ACIA Rx /Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.14 ELECTRICAL REQUIREMENTS

2.2.14.1
The front panel and chassis shall be connected to equipment ground.

2.2.14.2
A surge arrestor shall be provided between the AC+ and AC- for protection against powerline noise transients. The surge arrestor shall meet the following requirements:

1. Recurrent peak voltage:	**212 Volts**
2. Energy rating maximum:	**20 Joules**
3. Power dissipation, average:	**0.85 Watt**
4. Peak current for pulses less than 6 us:	**2000 Amperes**
5. Standby current:	**less than 1 mA**

2.2.14.3
Two 0.5 ohm, 10 watt wire-wound power resistors with a 0.2µH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68µF capacitor shall be added between AC+ and AC- coming off the 0.5 Ohm resistor going to the surge arrestors.

2.2.14.4
The AC power to the controller unit shall be supplied by a 3-conductor cable at least 3 feet in length. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.14.5
Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 1.59 mm diameter and 4.76mm high, minimum. The clearance between test points and other components shall be 6.35 mm, minimum.

2.2.15 M170E AUXILIARY BOARD

2.2.15.1
The M170E Auxiliary Board shall contain the RTCA Circuitry and the Identification Switches. (See Section 3 for the RTCA circuitry and the Identification Switch requirements.) The RTCA circuitry and the Identification Switches on the M170E Auxiliary Board shall be disabled when a Model 412C is installed. The M170 connector pins 71 and / or 72 shall provide a DC Ground path via the Model 412C Module (pins 69 & 70) to M170E connector (pins 71 & 72). A ground true present shall cause board feature disablement.

2.2.15.2
The M170E Auxiliary Board's PCB dimensions shall be identical to the Model 400 Modem except for the PCB edge connector dimensions.

2.2.15.3
The M170E Auxiliary Board's PCB connector shall be a PCB 36 / 72 and shall mate with the M170E connector.

CHAPTER 2 SECTION 3

MODEL 400 MODEM MODULE

2.3.1
The MODEM shall provide two-wire half duplex and four-wire full duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN / OUT.

2.3.2
The MODEM shall be compatable with Bell Standard 202S and comply with the following requirements:

2.3.2.1
Data Rate: 300 to 1200 baud modulations.

2.3.2.2
Modulation: Phase coherent frequency shift keying (FSK).

2.3.2.3
Data Format: Asynchronous, serial by bit.

2.3.2.4
Line and Signal Requirements: Type 3002 voice-grade, unconditioned.

2.3.2.5
ACIA and MODEM Interface: EIA - 232 Standards.

2.3.2.6
Tone Carrier Frequencies (Transmit & Receive): 1200 Hz (MARK) and 2200 Hz (SPACE) with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.3.2.7
Transmitting Output Signal Level: 0, -2, -4, -6 and –8 dB (at 1700 Hz) continuous or switch selectable.

2.3.2.8
Receiver Input Sensitivity: 0 to –40 dB.

2.3.2.9
Receiver Bandpass Filter: Shall meet the error rate requirement and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.3.2.10
Clear-to-Send (CTS) Delay: 12 (±2) ms.

2.3.2.11
Receive Line Signal Detect Time: 8 (±2) ms mark frequency.

2.3.2.12
Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

2.3.2.13
Soft Carrier (900 Hz) Turn Off Time: 10 (±2) ms.

2.3.2.14
MODEM Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

2.3.2.15
Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.3.2.16
Transmit Noise: Less than –50 dB across 600 ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.3.3
The MODEM power requirements are as follows:

Input Voltage	Maximum Current Consumption
+12 VDC	75 Milliamperes
-12 VDC	75 Milliamperes

2.3.4
Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data.

CHAPTER 2 SECTION 4

MODEL 412C PROGRAM MODULE

2.4.1 GENERAL REQUIREMENTS

2.4.1.1
A device shall be provided to prevent the module, when inserted upside down, from making contact with the modules' mating connector within the controller unit.

2.4.1.2
The module PCB Connector shall be provided with electrostatic discharge protection to prevent CMOS device damage.

2.4.1.3
The VMA / Phase 2 (E) Clock Signal (M/170 Pin 25) shall not be used in a memory device READ operation.

2.4.1.4
The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.

2.4.1.5
Address 700E, Bit 8 shall permanently Read as "1". This bit state is used to differentiate between past delivered Model 412/64 modules (Bit 8 decoded "0") and the Model 412C module.

2.4.1.6
The module PCB connector shall be a PCB 36/72P.

2.4.1.7
The module front panel shall be connected to Equipment Ground at M170 Pin 34.

2.4.1.8
All addressable devices shall be fully decoded.

2.4.1.9
All memory sockets shall be a 28 pin AUGAT #528/828 Series AG10DPC or equal.

2.4.2 FEATURE REQUIREMENTS

2.4.2.1 BUS INPUTS AND OUTPUTS

2.4.2.1.1
All data lines shall be tri-state buffered on the module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data output lines shall be disabled into a high impedance state and the data lines shall not source or sink more than 100 µA.

2.4.2.1.2
All addressed input lines shall load the bus by 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 ns.

2.4.2.2 MEMORY

2.4.2.2.1
Four numbered memory sockets shall be provided and fully decoded using the following method. The module shall be delivered with MEMORY SELECT #3 Configuration designated memory devices (OR EQUAL), address decode and jumpers.
2.4.2.2.2Device manufacturer is designated as INT-Intel, D-Dallas and HD-Hitachi. The sockets shall be decoded by block jumper selection as follows:

MEMORY SELECT	SOCKET ADDRESS RANGE AND DEVICE				JUMPER PATTERN		
	U1	U2	U3	U4	1	2	3
1	E000-FFFF INT2764A	C000-DFFF INT2764A	7010-7FFF DAL1225	1000-4FFF HD6264 OR HD62256	IN	IN	OUT
2	C000-FFFF INT128A	8000-BFFF INT128A	SAME	SAME	OUT	IN	IN
3	8000-FFFF	NOT ADRS	SAME	SAME *	OUT	OUT	IN
4	8000-FFFF INT27256A	3000-4FFF DAL1225	SAME	1000-2FFF SAME *	OUT	OUT	OUT

*** The pin #26 jumper pattern shall provide either address line 13 for the HD62256 device or tied HIGH for CS2 function in HD6264. Pin 27 shall be assigned to WE function.**

2.4.2.2.3
Jumper positions for Sockets U2 and U4 shall be provided to convert the sockets from an EPROM socket to a SRAM socket or vice versa. Jumper positions for Sockets U2, U3 and U4 shall be provided to convert the socket from a non-standby power socket to a standby power socket or vice versa. Sockets U2 and U3 shall be jumpered for non-standby power. Socket U4 shall be jumpered for standby power.

2.4.2.2.4
A Write Protect Circuit (WPC) shall be provided to prevent writing to SRAM memory during the Controller Unit MPU RESET Interrupt Line in a LOW State. A WRITE to ADDRESS 7000 shall be decoded and shall activate the WPC to place the R/W in a READ ONLY State. A subsequent WRITE to ADDRESS 7000 shall be decoded and shall deactivate the WPC allowing R/W function. The WPC state shall be brought out to Address 700E, Bit 7 ("1" State means "active"). The WPC power drain shall not exceed 40 µA at +5 VDC.

2.4.2.3
MODULE POWER SUPPLY

2.4.2.3.1
A power supply shall be provided onboard the module consisting of a DC Regulation Circuit, Standby Power and all necessary support circuitry.

2.4.2.3.2
A DC Regulator device with its circuitry shall be provided to reduce the +12 VDC to +5 VDC for module use. The Regulator shall have a minimum efficiency of 75% and provide +5 ±0.25 VDC from no load to full load with a maximum of 2% ripple.

2.4.2.3.3
Standby power shall be provided to holdup WPC, SRAM and RTCA circuits during a Model 170 Controller Unit Power Failure. A circuit shall be provided to sense the +12 VDC M/170 power line and switch to standby power when the line falls below +9 VDC. The standby power circuit shall switch off when the power line is greater than +11 VDC. The standby power shall be a standard "AA" cap terminal cell battery rated at a minimum of 1.6 Ampere-hours at 3.7 ±0.2 VDC. All module circuitry and devices shall not exceed a maximum power drain of 2 mA at 3.7 VDC on the Standby Battery.

2.4.2.3.4
The battery shall be delivered separate from the module. It shall not be used except for test loading check by the Contractor.

2.4.2.3.5
A battery holder for a "AA" battery shall be provided securely mounted to the back of the front panel. The holder shall have a TAB header type connector attached to the battery plus mounting terminal.

2.4.2.4 IDENTIFICATION SWITCH CIRCUITRY

2.4.2.4.1
Two identification switch packages and associated circuitry shall be provided. The switch packages shall be decoded at Address 7000 (features) and 7001 (locations). Each package shall have 8 SPST switch positions with each switch associated to a DATA Bit (Switch 1 to Bit 1 and so on). Switch ON shall denote bit state "1" to the 170 CPU and Switch OFF shall denote bit state "0" to the 170 CPU.

2.4.2.4.2
The Switch Package shall be a DIP slide type and shall have recessed switches to prevent accidental switching.

2.4.2.5
REAL TIME CLOCK AJUSTER (RTCA)

2.4.2.5.1
A RTCA shall be provided to adjust for missing RTC timing interrupts.

2.4.2.5.2
The RTCA shall be continuously powered and not affected by a controller unit power failure. RTCA accuracy shall be ±10 ppm at 25^0C. Integral devices incorporating RTCA features and functions may be used in lieu of individual components. The RTCA current drain shall not exceed 1.5 mA at +3.7 VDC.

2.4.2.5.3
The RTCA shall include a free running 60 Hz Pulse Generator (PG), a 24 bit binary counter counting 60 Hz pulses, 4 eight-bit buffer ports and port decode / PG interrupt logic. The PG shall trigger binary counter to increment on every input pulse, counting continuously until reset to 0 by its Reset Line. Bits 21, 22, 23 and 24 in an all "1"'s state shall cause that PG to be disabled (Binary Counter Bit 1 is the least significant bit).
2.4.2.5.4
The counter bits shall be continuously read out to 4 eight-bit buffer ports. The ports shall be addressed and bits assigned as follows:

CPU ADDRESS	PORT BITS	COUNTER BITS	COMMENTS
700A	This address shall normally READ (decode) "55 HEX". If the standby power supply fails or is removed, it shall decode "54 HEX". A WRITE to this address will RESET the RTCA Binary Counter.		
700B	1-6	1-6	READ Only
700C	1-6	7-12	READ Only
700D	1-6	13-18	READ Only
700E	1-6	19-24	READ Only

2.4.2.5.5
A SPST finger throw LOGIC switch shall be provided on the board to activate/deactivate standby power to the RTCA Circuitry. With the switch in the deactivated state the RTCA Circuitry shall present NO power drain to the standby power supply.

CHAPTER 2 SECTION 5

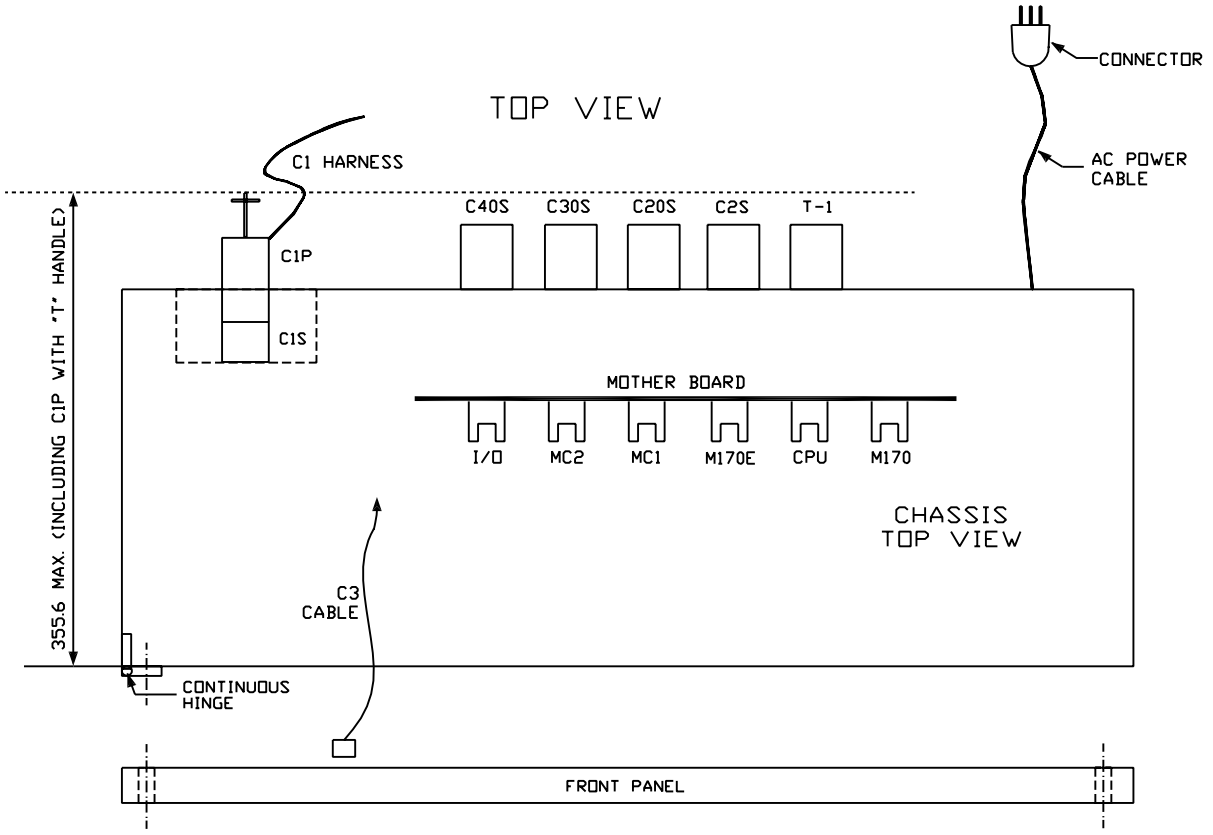
CHAPTER DETAILS

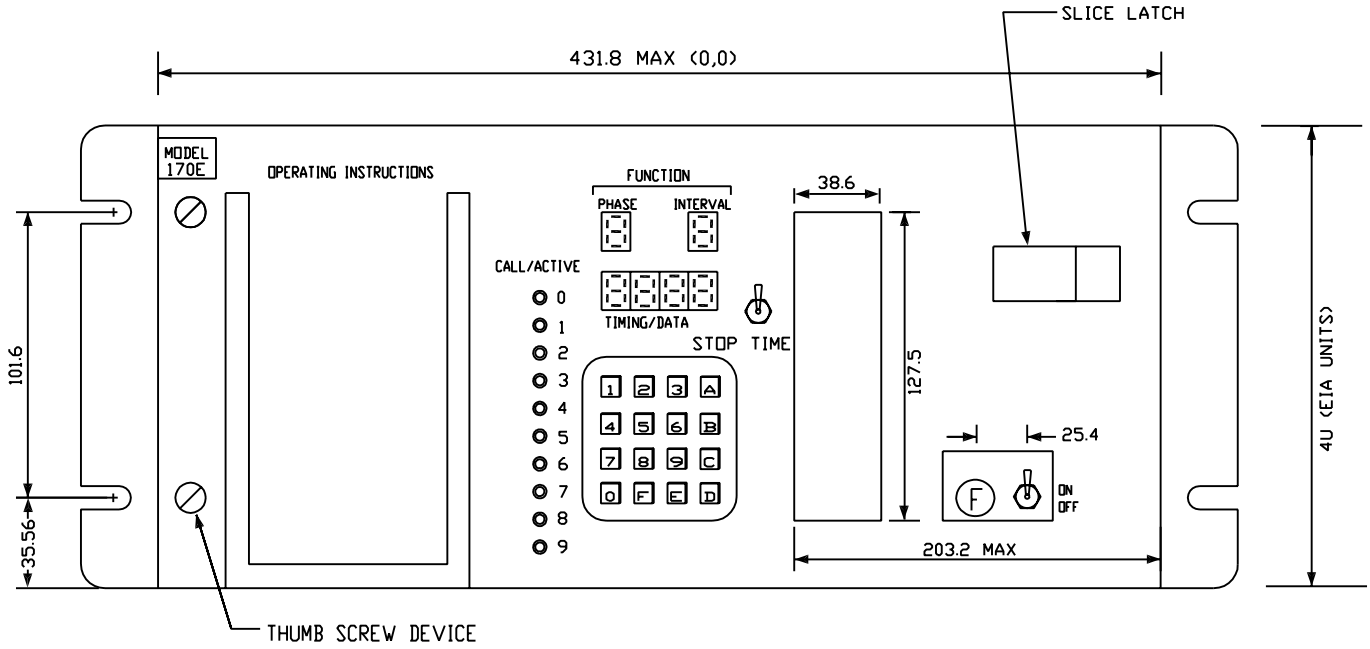
NOTES:

1. **All dimensions shall be in millimeters.**
2. **Program module' height and width dimensions are maximum.**
3. **C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.**
4. **All function under connector C2 & the terminal block T-1 are in reference to the MODEM**
5. **Detail Definitions:**

BL = BLANKING
CC = CHARACTER CONTROL OR STROBE
CD = CARRIER DETECT
CH = CHARACTER
CTS = CLEAR TO SEND
DP = DECIMAL POINT
LS = LEAST SIGNIFICANT
MS = MOST SIGNIFICANT
NA = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
NLS = NEXT LEAST SIGNIFICANT
NMS = NEST MOST SIGNIFICANT
P&I = PHASE AND INTERVAL
RTS = REQUEST TO SEND

MODEL 170E CONTROLLER UNIT DIAGRAM



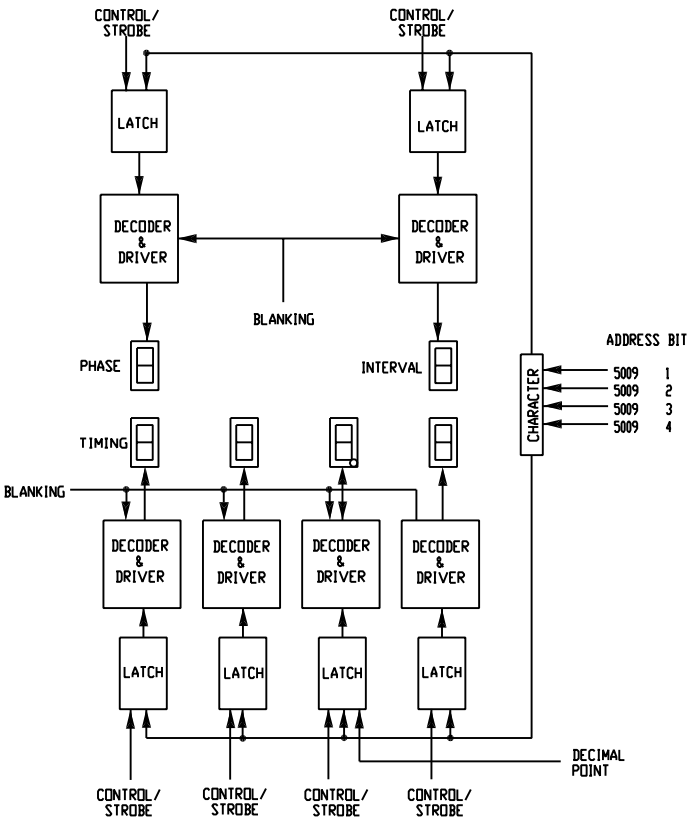


FRONT PANEL DISPLAY AND UNIT DETAIL

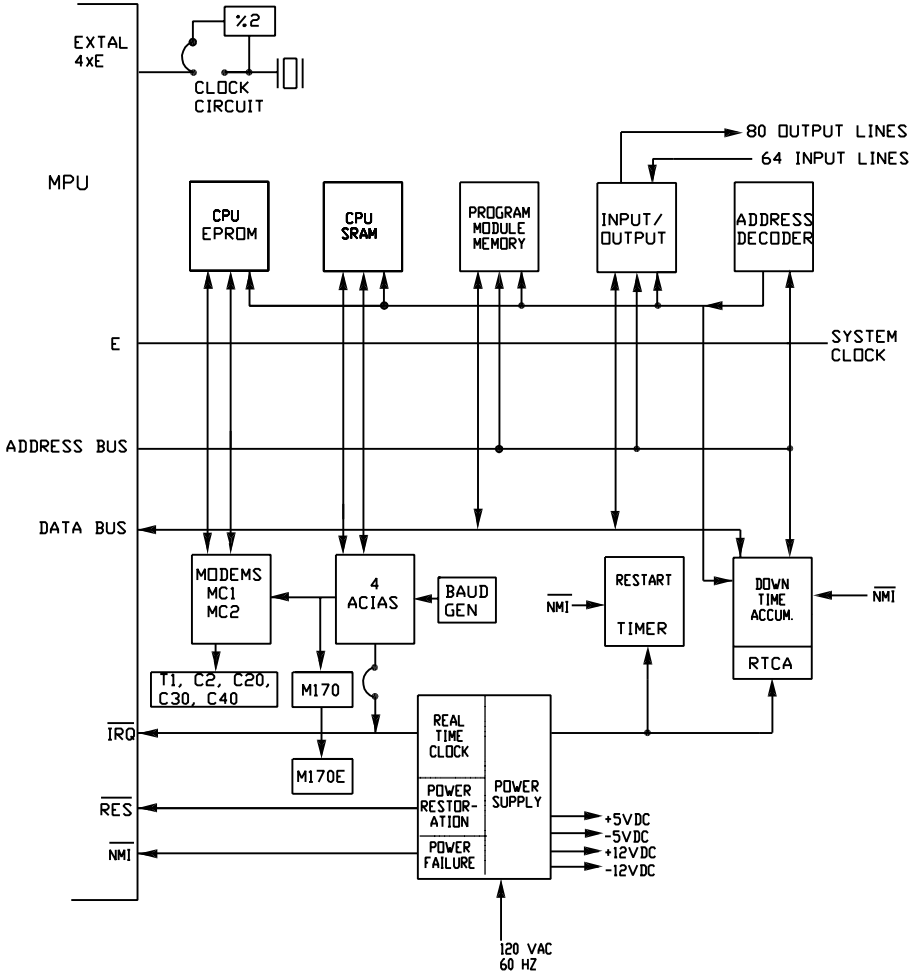
	TITLE: MODEL 170E CONTROLLER UNIT DIAGRAM	
	NO SCALE	
	TEES, NOV 19, 1999	2-5-1

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

FRONT PANEL DISPLAY BLOCK DIAGRAM



ORGANIZATION OF MODEL 170E CONTROLLER UNIT BLOCK DIAGRAM



TITLE:
MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

NO SCALE

TEES, NOV 19, 1999

2-5-2

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	
5001	1	39	5005	1	67	
5001	2	40	5005	2	68	
5001	3	41	5005	3	69	
5001	4	42	5005	4	70	
5001	5	43	5005	5	71	
5001	6	44	5005	6	72	
5001	7	45	5005	7	73	
5001	8	46	5005	8	74	
5002	1	47	5006	1	75	
5002	2	48	5006	2	76	
5002	3	49	5006	3	77	
5002	4	50	5006	4	78	
5002	5	51	5006	5	79	
5002	6	52	5006	6	80	
5002	7	53	5006	7	81	
5002	8	54	5006	8	82	
5003	1	55	5007	1		KEYBOARD CONTROL
5003	2	56	5007	2		KEYBOARD CH LS
5003	3	57	5007	3		KEYBOARD CH NLS
5003	4	58	5007	4		KEYBOARD CH NMS
5003	5	59	5007	5		KEYBOARD CH MS
5003	6	60	5007	6		STOP TIMING
5003	7	61	5007	7		NA
5003	8	62	5007	8		NA
5004	1	NA	5008	1		NA
5004	2	NA	5008	2		NA
5004	3	NA	5008	3		NA
5004	4	NA	5008	4		NA
5004	5	63	5008	5		NA
5004	6	64	5008	6		NA
5004	7	65	5008	7		NA
5004	8	66	5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40)

C2 SOCKET CONTACTS	FUNCTION	C2 SOCKET CONTACTS	FUNCTION
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data OUT
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND
F	-5VDC	P	NA
H	CD	R	NA

TERMINAL BLOCK T-1 ASSIGNMENTS

1. Audio IN
2. Audio IN
3. CD
4. RTS
5. Data IN
6. CTS
7. Data Out
8. Audio Out
9. Audio Out
10. DC GND

TITLE:

MODEL 170E INPUT ADDRESS

NO SCALE

TEES, NOV 19, 1999

2-5-3

OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	C3
5001	1	2	5006	1	83	
5001	2	3	5006	2	84	
5001	3	4	5006	3	85	
5001	4	5	5006	4	86	
5001	5	6	5006	5	87	
5001	6	7	5006	6	88	
5001	7	8	5006	7	89	
5001	8	9	5006	8	90	
5002	1	10	5007	1	91	
5002	2	11	5007	2	93	
5002	3	12	5007	3	94	
5002	4	13	5007	4	95	
5002	5	15	5007	5	96	
5002	6	16	5007	6	97	
5002	7	17	5007	7	98	
5002	8	18	5007	8	99	
5003	1	19	5008	1		CC-PHASE
5003	2	20	5008	2		CC-INTERVAL
5003	3	21	5008	3		CC-TIMING LS
5003	4	22	5008	4		CC-TIMING NLS
5003	5	23	5008	5		CC-TIMING MLS
5003	6	24	5008	6		CC-TIMING MS
5003	7	25	5008	7		CALL LT 8
5003	8	26	5008	8		CALL LT 9
5004	1	27	5009	1		CH-LS
5004	2	28	5009	2		CH-NLS
5004	3	29	5009	3		CH-NMS
5004	4	30	5009	4		CH-MS
5004	5	31	5009	5		DP
5004	6	32	5009	6		BL-P&I
5004	7	33	5009	7		BL-TIMING
5004	8	34	5009	8		NA
5005	1	35	500A	1		CALL LT 0
5005	2	36	500A	2		CALL LT 1
5005	3	37	500A	3		CALL LT 2
5005	4	38	500A	4		CALL LT 3
5005	5	100	500A	5		CALL LT 4
5005	6	101	500A	6		CALL LT 5
5005	7	102	500A	7		CALL LT 6
5005	8	103	500A	8		CALL LT 7

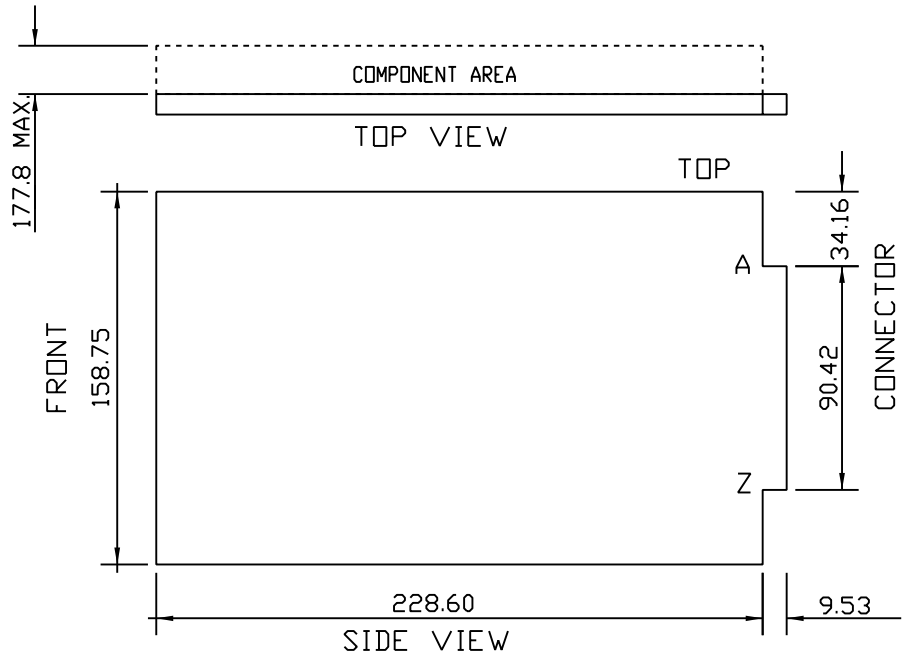
TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3

NO SCALE

TEES, NOV 19, 1999

2-5-4

MODEL 400 MODEM MODULE



MODEL 400 MODULE CONNECTOR ASSIGNMENT

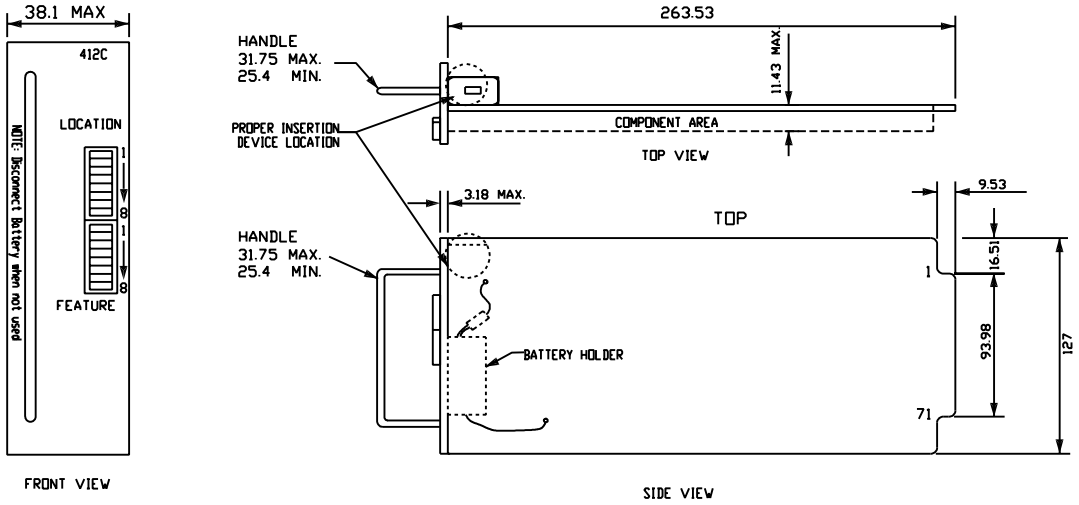
COMPONENT SIDE		CIRCUIT SIDE	
CONTACT	MODEL 400 FUNCTION	CONTACT	MODEL 400 FUNCTION
1	NA	A	DC GROUND
2	AUDIO INPUT	B	DC GROUND
3	AUDIO INPUT	C	12 VDC
4	NA	D	12 VDC
5	NA	E	-12 VDC
6	NA	F	-12 VDC
7	NA	H	NA
8	NA	J	NA
9	NA	K	CARRIER DETECT
10	NA	L	REQUEST TO SEND
11	NA	M	DATA INPUT
12	NA	N	CLEAR TO SEND
13	NA	P	DATA OUTPUT
14	NA	R	NA
15	NA	S	NA
16	NA	T	NA
17	NA	U	NA
18	NA	V	NA
19	NA	W	NA
20	NA	X	AUDIO OUTPUT
21	NA	Y	AUDIO OUTPUT
22	NA	Z	NA

TITLE:

MODEL 400 MODEM MODULE

	NO SCALE	
	TEES, NOV 19, 1999	2-5-5

MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E



M170, M170E, AND 412C
PROGRAM MODULE CONNECTOR ASSIGNMENTS

CIRCUIT SIDE		COMPONENT SIDE		M170 ONLY
FUNCTION	PCB CONNECTOR		FUNCTION	NOT REQUIRED BY 412C
A0	1	2	A1	
A2	3	4	A3	
A4	5	6	A5	
A6	7	8	A7	
A8	9	10	A9	
A10	11	12	A11	
A12	13	14	A13	
A14	15	16	A15	
$\overline{D0}$	17	18	$\overline{D1}$	
$\overline{D2}$	19	20	$\overline{D3}$	
$\overline{D4}$	21	22	$\overline{D5}$	
$\overline{D6}$	23	24	$\overline{D7}$	
$\overline{VMA}$ / Q2(E)	25	26	NA	RES
READ/WRITE	27	28	NA	NMI
NA	29	30	NA	RDT
NA	31	32	NA	
NA	33	34	EQUIP. GND	
NA	35	36	NA	RTS ACIA 4
NA	37	38	NA	CTS ACIA 4
NA	39	40	NA	DCD ACIA 4
NA	41	42	NA	TXD ACIA 4** (SEE NOTE)
NA	43	44	NA	RXD ACIA 4** (SEE NOTE)
NA	45	46	NA	
NA	47	48	NA	
NA	49	50	NA	
NA	51	52	NA	
NA	53	54	NA	
NA	55	56	NA	
NA	57	58	NA	
12 VDC	59	60	12 VDC	
-12 VDC	61	62	-12 VDC	
	KEY			
-5 VDC	63	64	-5 VDC	
5 VDC	65	66	5 VDC	
5 VDC	67	68	5 VDC	
GND	69	70	GND	
GND	*71	*72	GND	

*PINS 71 & 72 ON M170 & M170E CONNECTORS SHALL BE COMMONED. PINS 71 & 72 ON THE MODEL 412C SHALL BE TIED TO PINS 69 & 70.

**RELATIVE TO THE ACIA

TITLE:
MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E

NO SCALE

TEES, NOV 19, 1999

2-5-6

CHAPTER 3

SPECIFICATIONS FOR AUXILIARY CABINET UNITS

TABLE OF CONTENTS

CHAPTER 3, SECTIONS 7, 8, 9 AND 10 ARE FOR ITS PROTOTYPE PROCUREMENT AND REVIEW ONLY.

CHAPTER 3 SECTION 1

GENERAL REQUIREMENTS

3.1.1 MODELS 200 AND 204 GENERAL

3.1.1.1
The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements. Where electrical isolation is the only requirement, plastic insulation material can be used in lieu of metal.

3.1.1.2
The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw head end (Slotted or Phillips) shall be used.

3.1.1.3
The unit shall be so constructed that no live voltage is exposed. A handle shall be attached to the front panel for insertion or removal from the unit mating connector.

3.1.1.4
The unit shall be so constructed that its lower surface shall be no more than 52.34 mm below the centerline of the connector and no part shall extend more than 22.86 mm to the left or 27.94 mm to the right of the connector centerline.

3.1.1.5
Continuous edge guides shall be provided on the unit.

3.1.1.6
Each switch shall be capable of switching any Current from 0.050 to 10.0 Amperes (AC) load with power factor of 0.85 or higher.

3.1.1.7
Each switch shall be designed for a minimum of 300 Million operations while switching a tungsten load of 1000 Watts at 70 degrees C. Switch isolation between DC input and AC output circuit shall be at least 10,000 meg-ohms at 2000 VDC.

3.1.1.8
Unit indicators shall be vertically centered on the front panel with indicators positioned no more than 25.3 mm from said center.

3.1.2
MODEL PLUG CONNECTORS SHALL BE:

Model 200	**BEAU P 5412 - LAB or equal**
Model 204	**BEAU P 5406 - LAB or equal**

CHAPTER 3 SECTION 2

MODEL 200 SWITCH PACK UNIT

3.2.1
The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches. Each switch shall open or close a connection between applied power and external load.

3.2.2
A Ground True Controller Unit Input (0 to 6 VDC) shall cause the switch to energize and a Ground False (16 VDC or more) shall cause it to de-energize, State transition shall occur between 6 and 16 VDC. The input shall not sink more than 20 ma or be subjected to more than 39 VDC. The input shall have reverse polarity protection.

3.2.3
With all switches on, the unit shall not draw more than 60 ma at +16 VDC or more from the +24 VDC cabinet supply.

3.2.4
Each switch shall have an OFF state dv/dt rating of 100 V/μs or better. Each switch shall be isolated so that line transients or switch failure shall not alter the controller unit.

3.2.5
The unit front panel shall have an indicator on the input to each switch. The indicator shall be labeled or color-coded "Red"-top switch, "Yellow"-middle switch, and "Green"-bottom switch. The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned 25.4 mm above and below.

3.2.6
The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15,000 ohms when the switch is in open state. When the switch is in off state the output current through the load shall not exceed 20 mA peak.

CHAPTER 3 SECTION 3

MODEL 204 - FLASHER UNIT AND

MODEL 205 – FLASH TRANSFER RELAY UNIT

3.3.1 MODEL204 FLASHER UNIT

3.3.1.1
The FTR shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The unit's function is to alternatively open and close connections between applied power and external load.

3.3.1.2
The unit shall generate its own internal DC power from the AC Line.

3.3.1.3
The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.

3.3.1.4
Each switch shall have an OFF state dv /dt rating of 200 V/μs or better.

3.3.1.5
An indicator showing the switch's output state shall be provided.

3.3.1.6
Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.

3.3.1.7
A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8). The arrestor shall meet the following requirements:

Recurrent Peak Voltage	**212 Volts**
Maximum Energy Rating	**50 Joules**
Average Power Dissipation	**0.85 Watts**
Peak I for pulses less than 6 us	**2000 Amperes**
Standby I	**less than 1 mA**

3.3.2 MODEL 205 FLASH TRANSFER RELAY UNIT

3.3.2.1
The relay unit shall be of electromechanical type, designed for continuous duty:

3.3.2.2
Each unit shall be enclosed in a removable, clear plastic cover. The manufacturer name, its electrical rating, and part number shall be placed on the cover. They shall be durable, permanent and readily visible.

3.3.2.3
Each unit shall be provided with DPDT contacts. The contact points shall be of fine silver, silver alloy or a superior alternate material. Contact points and arms shall be capable of switching 20 Amperes or 1 Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation. The points and arms shall be able to withstand 0.1 DA or !0 Gs, 10 –55 HZ without contact chatter.

3.3.2.4
The relay coil shall have a power consumption of 2.0 Volt - Ampere maximum.

3.3.2.5
Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 ms.

CHAPTER 3 SECTION 4

MODEL 206 T170 POWER SUPPLY UNIT

3.4.1
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.4.2
The unit shall provide +24 VDC to the cabinet files. The unit shall be of ferro-resonant design. It shall have no active components and conform to the following requirements:

3.4.2.1
Input Protection - Two 0.5 ohm, 10-watt wire-wound power resistors with a 0.2 µh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 µf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.4.2.2
Line and load regulation shall meet the power supply range for +24 VDC (23.0 to 26 VDC). This includes ripple noise; from 90 to 135 VAC at 60 Hz., plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 30 degrees C above ambient.

3.4.2.3
Design Voltage - +24 +/- 0.5 VDC at full load, 30 degrees C, 115 VAC incoming after a 30-minute warm-up period.

3.4.2.4 Full Load Current 5 AMPS each for +24 VDC, minimum.

3.4.2.5 Ripple Noise - 2 volts peak-to-peak and 500 millivolts RMS at full load.

3.4.2.6 Efficiency - 70% minimum.

3.4.2.7 Circuit capacitors shall be rated for 40 volts minimum.

3.4.3
The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

CHAPTER 3 SECTION 5

MODEL 208 T170 MONITOR UNIT

3.5.1
The Model 208 Monitor Unit shall reliably sense and cause a relay output contact (FAILED STATE) when monitoring the following:

1. **A WDT Timeout Condition**
2. **Cabinet +24 VDC Power Supply below specified threshold**

3.5.2
WatchDog Timer Requirements

3.5.2.1
WDT Circuitry shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT Circuitry shall sense any line state change and the time between the last change. No state change for 1.5 ± 0.1 seconds shall cause a FAILED state. The timer shall reset at each state change in a NON FAILED state.

3.5.2.2
Only the Unit Reset or a WDT inactive due to the voltage sense shall reset the WDT from a FAILED state.

3.5.2.3
A FAILED state caused by the WDT shall illuminate a front panel indicator light labeled "WDT ERROR". The indicator shall remain ON until Unit Reset Issuance.

3.5.2.4
The WDT Circuitry shall sense the incoming VAC Line and when the voltage falls below 98 ± 2 VAC for 50 ± 17 ms shall inhibit the WDT Function. When the WDT Circuitry senses the incoming VAC Line rise above 103 ± 2 VAC for 50 ± 2 ms the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active Settings shall be a minimum of 3 Volts.

3.5.3
Power Supply Monitor Requirements

3.5.3.1
The monitor unit shall sense the Cabinet +24 VDC Power Supply Output Voltage. Voltages sensed at +18 VDC or below for a duration of 500 ms or longer shall cause a FAILED state. Voltages sensed at +22 VDC or above shall NOT cause a FAILED state. Voltages sensed below +22 VDC for a duration of 200 ms or less shall NOT cause a FAILED state. All timing and voltages conditions other than those specified above may or may not cause a FAILED state.

3.5.3.2
A FAILED state caused by sensing the power supply shall illuminate a front panel indicator light labeled "VDC FAILED". The indicator shall remain ON until Unit Reset.

3.5.3.3
Only Unit Reset shall reset the power supply sense circuitry from a FAILED state.

3.5.4
FAILED State Output Circuits
An electro-mechanical relay shall be provided to switch an output circuit during a FAILED state. The relay coil shall be energized in a NON FAILED State. The relay contacts shall be rated for a minimum of 3 amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.5.5
Monitor Unit Reset
A momentary SPST CONTROL switch labeled "RESET" shall be provided on the unit front panel to reset the monitor unit circuitry to a NON FAILED state. The switch shall be so positioned on the front panel that the switch can be operatied while gripping the front panel handle.

3.5.6
The unit shall be provided with provision to drive an external NE2H light through a 56 KOhm, 1/2 Watt series restor (resident on unit).

3.5.7
The PDA #3 WDT Reset Input shall not be sensed by the unit.

3.5.8
The output relay CONTACT FOR FAILED STATE shall be OPEN

CHAPTER 3 SECTION 6

MODEL 210 T170 MONITOR UNIT

3.6.1
The Monitor Unit shall sense the following conditions and cause a FAILED STATE should any of the conditions exist:

1. **The cabinet +24 VDC power supply below the voltage threshold.**
2. **The WDT Timeout Condition.**
3. **Conflicting field Output Circuit ON Condition.**

3.6.2
See Chapter 3, Section 5 Model 208 Monitor Unit for requirements on Power Supply Monitoring, Watchdog Timer, FAILED State Output Circuits and Monitor Unit Reset.

3.6.3
Conflict Monitoring
The monitor shall sense up to 16 Channels for conflict (32 field outputs of Green and Yellow). The Green and Yellow are Logically ORed together. The associated cabinet output file assignment or operator selected output switches shall determine channel assignment.

3.6.3.1
All monitored field output voltages shall be measured as true RMS responsive (up to 3 KHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 2 cycles. If digital means are used in calculating RMS, a min. of 2 samples shall be taken per alternation.

3.6.3.2
Sensed conflicting field output voltages 25 VAC or greater for a duration of 500 ms or longer shall cause a FAILED state. Sensed conflicting field output voltages between 15 VAC or less OR any voltage having a duration of 200 ms or less shall NOT cause a FAILED states. Sensed conflicting field output voltages between 15 and 25 VAC and for durations between 200 and 500 ms may or may not cause a FAILED state.

3.6.3.3
The conflict monitoring circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.

3.6.3.4
A FAILED state caused by sensing voltage conflicts shall be reset only by the Unit Reset.

3.6.3.5
Sixteen indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a FAILED state unless unlatched by Unit Reset or a unit loss of power during said FAILED state.

3.6.4
Conflict Programming Card

3.6.4.1
A plug-in PCB Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place all output channels being monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed the channels shall be defined as non-conflict.

3.6.4.2
A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin the yellow inhibit common shall disable sensing the said channel yellow.

3.6.4.3
The programming card shall intermate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provided a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flushed with the unit's front panel.

3.6.4.4
Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

3.6.5
A front panel indicator labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset Issuance.

3.6.6
The output relay contact for FAILED State shall be "CLOSED".

3.6.7

A second output circuit (STOPTIME controller input) shall be provided to sink a NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 ma at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from souring power into the controller unit.

3.6.8

An internal SPST LOGIC toggle switch shall be provided on the Model 210 Monitor Unit to activate the WDT function. When the switch is ON the WDT Circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.

3.6.9

The Front Panel RESET Switch shall be tied to the External Test Reset Input Line (Pin Z). The External Line shall be optically isolated from internal circuitry.

CHAPTER 3 SECTION 7

MODEL 212 ITS CABINET MONITOR UNIT (CMU)

GENERAL

3.7.1.1
The CMU is the principle part of the ITS Cabinet Monitoring System (see Chapter 7 Specifications). It is resident in the Power Distribution Assembly (#5 or #6). The CMU's role is to query various cabinet conditions and, if the application requires action, the CMU shall transfer control from the ATC Controller to a safe control mode (Signalized Intersection or Ramp Metering). Many applications do not require any action, only data gathering and report back to the ATC. In fact, some applications require no monitor at all (CCTV and HAR).

3.7.1.2
The CMU shall be composed of an MPU, memory devices including non-volatile memory, communications circuitry to interface with Serial Buses #1 & #3 and Frout Panel / Laptop, Front Panel Indicators, Front Panel Communication Connector and a DATAKEY Memory Device. The Operating Program shall be resident in the Non-volatile memory. The DATAKEY Memory shall possess the conditions and function selections of the Unit. A list of inclusive unit operational monitoring functions shall be as follows

The Cabinet Power Supplies (LFSA)
Conflicting Channels (LFSA)
Serial Bus Error (LFSA)
Message 62 (LFSA)
Monitor Error (LFSA)
Multiple Channel Indications (LFSA)
Lack of Channel Indications (LFSA)
Short and Long Yellow (LFSA)
Individual FTR Coil Failed (LFSA)
Logic Signal Error (LFSA)
Police and PDA Flash Switch Action (LFSA)
Door Switches
Circuit Breakers and Mercury Contact Status
Flasher Unit Output Status
AC line level sense

LFSA - Latched Failed State Action

3.7.1.3
Only Unit Reset shall RESET from LATCHED FAILED STATE ACTION.

3.7.1.4
The Model 212 Unit VERSION is programmed to provide one, part or all FUNCTIONS (F):

FUNCTIONS	VERSIONS		
	A	B	C
Cabinet Power Supplies	F	F	F
Conflicting Phases	-	F	F
Serial Bus #1 Errors	F	F	F
Message 62	F	F	F
Monitor Error	F	F	F
Multiple indications on	-	F	-
Lack of indicators	-	F	-
Short and long Yellows	-	F	-
Individual FTR Coil Error	F	F	F
Logic Signal Error	F	F	F
Police and/or PDA FLASH Switch	F	F	F
Door Switches	F	F	F
Circuit Breakers & Mercury Contactor Status	F	F	F
Flasher Unit Output Error	F	F	F
A C Line Level Sense	F	F	F

Model 212 Version A – Ramp Metering Application
Model 212 Version B – Traffic Signal Application, **
Model 212 Version C – Traffic Signal Application, Agency "CAL"

**** Care should be taken in use of the functions called out here. Because they are listed and described, doesn't mean they are recommended for use. Two words are paramount, SAFETY and LIABILITY. The user excepts the responsibility. Note Version C as an example.**

FUNCTIONS - DETAILED DISCRIPTIVE

3.7.2.1
CABINET POWER SUPPLIES - The CMU shall sense the Cabinet +24 VDC and +12 VDC power supply sources. Voltages at or greater than +22 VDC and +11 VDC shall NOT cause a LFSA. Voltages at or less than +18 VDC and +9 VDC for 500ms or longer shall cause a LFSA. If the sensed voltage is less than +22 or +11 VDC for duration of 200 ms or less, the CMU shall NOT cause a LFSA. All other timing or voltage conditions may or may not cause LFSA.

3.7.2.2
CONFLICTING CHANNELS -The CMU shall be designed to monitor cabinet AMU Voltage One States sent back by the AMUs. If the associate channel matrix (in DATAKEY) designates the channels in conflict, the CMU shall set LFSA. *The CMU*

receives a message from the ATC Controller specifying the channel output for each switchpack. This information represents the status of the intersection control data. The intersection control data shall be compared to the (DATAKEY) channel matrix to determine conflict. Additionally the control data shall be compared to the AMU Voltage One States. If the Voltage One States do not agree with the control data the CMU shall be set to LFSA. **The CMU shall be designed to monitor twenty four (24) channels composed of a assigned switch pack from the AMUs and eight (8) additional virtual channels formed by any 3 outputs. This provides 32 channels of monitoring. There shall be a Yellow Inhibit feature provided to selectively inhibit yellow channel inputs on a per channel basis.**

3.7.2.3
SERIAL BUS ERROR - The CMU communicates with both Serial Bus (SB) #1 and #3. In SB #1 the CMU is a Responder (polled by the ATC). In SB #3 it is the Commander (polling the Output Assemblies AMU).

3.7.2.3.1
Bus #1 Error: Communications between the ATC and CMU has ceased for 2 sec. or more.

3.7.2.3.2
Bus #3 Error – No Comm. between the CMU & AMU for 300 ms shall cause a LFSA.

3.7.2.4
MESSAGE 62 - The ATC shall send a Message 62 via Serial Bus #1. The CMU upon receipt shall react by setting LFSA. The ATC Response shall note FAILED Status and what caused the State.

3.7.2.5
MONITOR ERROR - A fault is detected within the operation of the CMU. The CMU shall be provided with a resident series of self-check diagnostic capabilities. The CMU shall contain provisions to verify all memory elements on Power Up and at least 10 times per second thereafter. When a fault is detected, the LFSA shall be set.

3.7.2.5.1
RAM Diagnostic: This test shall verify that all RAM elements are operating correctly. Patterns shall be written to RAM. Each Write shall be followed by a Read to verify that it contains the written pattern.

3.7.2.5.2
ROM Diagnostic: This test shall verify that the Operation System ROM(s) contain the proper program. The routine shall perform a check on each ROM and make a comparison with a preprogrammed check value.

3.7.2.5.3
Non-Volatile Memory Diagnostic: This test shall verify whether the Non-Volatile Memory contains valid data and that the data has not changed since the last write. The routine shall perform a check on each Non-Volatile Memory Element and make a comparison with a preprogrammed check value.

3.7.2.6
MULTIPLE CHANNEL INDICATIONS - Simultaneous indications of Green, Yellow or Red field outputs (AMU Current 1) on a single channel for 500 ms and greater, shall cause the CMU to set LFSA. Multiple Outputs shall be selected on a per channel basis.

3.7.2.7
LACK OF CHANNEL INDICATIONS - No active field outputs AMU Current 1 on a single channel (Green/Walk, Yellow, Red/Don't Walk) for 1300 ms and greater, shall cause the CMU to set LFSA. Lack of Output shall be selected on a per channel basis.

3.7.2.8
SHORT & LONG YELLOW - The absence of a minimum period (2.7 +/- 0.1 sec.) or maximum period (6.7 +/- 0.1 SEC) of active yellow field output during a green to red sequence, shall cause the CMU to set LFSA. Yellow Error shall be selected on a per channel basis.

3.7.2.9
INDIVIDUAL FTR COIL FAILED – The CMU shall monitor the AMU FTR Coil States. If all coils are not the same state, the CMU shall set the LFSA.

3.7.2.10
LOGIC SIGNAL FAIL – The CMU has three system logic lines presented to it by the ATC; LINESYNC, POWER DOWN and NRESET. The 60 HZ 5 Volt Square Wave LINESYNC originates in the ATC Power Supply synchronized off the 60 HZ incoming VAC Line (transition points at 120 and 300 degrees). It shall continue until NRESET goes LOW (GROUND TRUE) and begin when NRESET goes HIGH. POWER DOWN goes LOW at Power Failure and transition HIGH at Power Restoration. NRESET goes LOW 525 +/- 25ms after POWER DOWN goes LOW and HIGH 225 +/- 25ms after POWER DOWN transitions HIGH.

3.7.2.10.1
The CMU shall monitor the three lines matching states denoted below and if operational conditions are met, shall set the unit to LFSA.

NRESET is HIGH and LINESYNC is LOW
NRESET is LOW and LINESYNC is HIGH
NRESET is LOW and POWER DOWN is HIGH
NRESET is HIGH and POWER DOWN Transitions Low for 550 ms

NRESET Transitions HIGH and 99 VAC or more, but NO COMM on Serial Bus #1 for 2 Seconds or more.

3.7.2.11
POLICE AND PDA FLASH SWITCH SET TO FLASH – the CMU shall monitor the two switch settings and set the LFSA if either is set to LFSA.

3.2.12
DOOR SWITCHES – The Cabinet has Front and Rear Doors. Each Housing #1 or #2 Door (or Housing #3 left side doors) has a switch which is Normally Closed when the Door is Open. The door states shall be sensed by the monitor and reported to the ATC via Serial Bus #1. The Front sensed door in a closed condition with the CMU out shall set to LFSA.

3.7.2.13
CIRCUIT BREAKER and MERCURY CONTACTOR STATUS – The Circuit Breaker tripped (any of the Eight breakers) shall be monitored by the CMU and reported back to the ATC. The Mercury Contactor status upon request shall be reported back to the ATC

3.7.2.14
FLASHER UNIT OUTPUT FAILED – The AMU shall sense the incoming four Flasher Unit circuits in the Output Assemblies. The CMU shall monitor all states collected by the AMUs. If anyone of the lines is down (NOT Operating), this shall be monitored and the state sent back to the ATC. No action shall be taken since the malfunctioned condition is normally sensed during Normal Operation.

3.7.2.15
AC LINE LEVEL SENSE – The CMU shall sense the Raw Protected AC Line Voltage +/- 1 Volt upon command by the Serial Bus #1 Message 64.

3.7.3
POWER AND CIRCUIT REQUIREMENTS

The CMU shall be operational over the voltage range of from 85 to 135 VAC. Assuming no Logic Error FAILED Condition exists and LINESYNC and NRESET transition to LOW, the CMU shall set a NON-LATCHED FSA for the system during ATC normal power down period. The CMU shall monitor LINESYNC and NRESET for transition to HIGH. At transition point and no LFSA condition, the CMU shall cease NON-LATCHED FSA returning to ATC Control and monitoring for set functions. If LATCHED FSA before Power Down, the CMU shall return to LFSA. This assumes Traffic Signal and Ramp Metering Applications.

3.7.3.2
The CMU shall not use the Cabinet + 24VDC Power Supply to run any of its internal Circuitry. The external RESET and +24VDC Monitor Input Circuits shall

be optically isolated from the internal CMU power supply and shall be conditioned to provide proper sense Circuit operation throughout the operating range.

3.7.3.3
Power restoration after a power failure shall not result in resetting the CMU. The CMU once triggered shall remain in that state until a Reset is issued. Reset is issued only by the Front Panel Reset Switch or by the External Test Reset input.

3.7.3.4
At power up the CMU shall delay monitoring the communication between the ATC and the CMU for at least 5 seconds then the CMU shall set LFSA.

3.7.3.5
A WATCHDOG Circuit shall be provided to scan the CMU Controller Unit every 100 ms. If the controller unit output doesn't change for 1 second, the WDT shall Reset the CMU Controller. The WDT shall be enabled upon NRESET going HIGH and disabled at CMU shut down.

FAILED STATE OUTPUT CIRCUIT

3.7.4.1
An electro-mechanical relay shall be used to provide the FAILED STATE output Circuit. The relay contacts shall be normally Closed (NON-FAILED STATE). In a FAILED state (relay coil de-energized), the contacts shall be Open. The function of this output Circuit is to initiate FAILED STATE operation within the cabinet and transfer field Circuits from the switch pack outputs to the flash bus during a FAILED STATE.

3.7.4.2
The relay contacts shall be rated for a minimum of 3 amperes at 120 V ac and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.7.4.3
Latch State: Once the Monitor is LATCHED in a fault condition for any reason, it shall REMAIN LATCHED, even through a power fail/recovery, until a UNIT RESET is issued by the front panel reset switch, or by the external test reset line.

3.7.4.4
Insertion / Removal Of Unit: It shall be possible to insert and remove the Monitor Units while the cabinet is energized without placing the cabinet into Flash operation provided that the cabinet door remains open.

3.7.4.5
The External Test Reset Input line and Front Panel RESET Switch shall reset the MU Circuitry to a Non-FAILED STATE and restore normal monitoring operation. It shall be optically isolated from the internal Circuitry. A reset issuance by either

source (Unit Reset) shall be triggered by only the leading edge of the input signal (this will prevent a constant reset due to either a switch failure or a constant external input).

FRONT PANEL DEVICES

3.7.5.1
The CMU Front Panel shall be provided with indicators, Front panel Communications Connector and a momentary RESET Switch. The switch and the External RESET line shall form the UNIT RESET.

3.7.5.2
The following indicators shall be provided (Top to Bottom):

Conflict LFSA	**- ON is LFSA**
Cabinet Power Supplies Error	**- ON is LFSA**
Serial Bus Error	**- ON is LFSA**
Lack of Indication	**- ON is LFSA**
Multiple Channel Indicator	**- ON is LFSA**
Logic Signal Fail	**- ON is LFSA**
Monitor Power Supply Error	**- Failed is blank & ON is operation**
Monitor LFSA	**- ON is LFSA**
Other	**- ON is LFSA**

3.7.5.3
A DB 9 Connector shall be provided for Laptop connection. The CMU shall provide EIA 232 TX / RX Drivers and receivers with Pin2- RXD, Pin 3 –TXD and Pin 5 – DC Ground assigned. The function report format available for the Serial Bus #1 shall also read out to the DB Serial Port. Pin A22 is the CMU Relay Output status pin. When the relay is closed, the cabinet is in the normal operating mode (Red, Yellow, Green). When the relay is de-energized (contacts open), the system goes to a flashing mode. The CMU uses the relay to control the following functions: Conflict Flash, Start-u-

MONITOR UNIT DATAKEY PROGRAMMING

3.7.6.1
A Unit Operational Program shall use the DATAKEY to set the function selection, function action and report processing and storage. The Address/Function Memory Map is as follows:

ADDRESS	**ASSIGNMENT**
000000 to 000001dec	**Monitor Function Setting CheckSum**
000002 to 000005	**Channels Assigned 0102030405060708**

0910111213141516
1718192021222324
2526272829303132

000006 to 000030 **Virtual Channels 25 to 32 Assignments**
Channel 25 Red to assigned SP "X" L S "X'
Channel 25 Yellow to assigned SP "x"LS "x"
Channel 26 green to assigned SP "x" LS "x'
This shall continue on to Channel 32

000031 to 000039 **Not Assigned**

000040 to 000059 **Function Selection - Functions 1 to 15 active if NON 0**
Addr 40 is Function 1. Addr 55 to 59 Not Assigned

000060 to 000192 The next 33 blocks of 4 Bytes are assigned to Conflict Monitoring. Block 1 is 32 Channels of Yellow Inhibit, lBit/Channel in Logic "1"= Channel Yellow Inhibit. Blocks 2 to 33 associate with 1 to 32 channels and the channels there are in conflict with. Again Logic "1" equals a conflicting channel.

000192 to 000199 **Not Assigned**

000200 to 000203 Multiple Indication Channel Selection
A block of four bytes with the bits associated to each channel for per channel selection

000204 to 000207 **Lack of Indication Channel Selection**
Same as Multiple Indication

000208 to 000211 **Short/ Long Yellow Channel Selection**
Same as multiple Selection

000212 to 004999 **Not Assigned**

005000 to Memory top Error/Status Reports logged in sequential order and in ASCI II. The Time Stamp block is the latest sent by the ATC in Serial Bus #1 Address 15, Message 61. The Report is common to the Time Stamp data. Thereafter, the data is unique to the function. Serial Bus #1 Address 15 Message 62 shall request the report response and set or clear the report area. The report response message shall be no longer than 30 Bytes.

Example:

"REPORT LAYOUT"
Addr 5000 BYTE 1 Header Symbol
BYTE 2 Header Symbol

Report Number Digit One
Report Number Digit Two
Report Number Digit Three
BYTE Count Digit One
BYTE Count Digit Two
Function Error Number (assume 2 Conflict)
Function Error Number Digit Two
Time Stamp "Day of Year Digit One
Time Stamp "Day of Year Digit Two
Time Stamp "Day of Year Digit Three'
Time Stamp "Hour Digit One"
Time Stamp "Hour Digit Two'
Time Stamp "Hour Digit Two"
Time Stamp "Minute Digit One'
Time Stamp " Minute Digit Two'
Time Stamp ' Second Digit One"

BYTE 19 Time Stamp "Second Digit Two"

“Unique Function Data”

BYTE 20 Conflict Channel 1 Digit One
Conflict Channel 1 Digit Two
Conflict Channel 1 Color (G or Y)
Conflict Channel 2 Digit One
Conflict Channel 2 Digit Two
Conflict Channel 2 Color (G or Y)
Conflict Channel 6 Digit One
Conflict Channel 6 Digit Two

BYTE 28 Conflict Channel 6 Color (G or Y)

Addr 5030 Start of next report

CHAPTER 3 SECTION 8

MODEL 214 - ITS AUXILIARY MONITOR UNIT (AMU)

3.8.1 GENERAL

The AMU shall be provided resident in each of the Output Assemblies unless otherwise called out. The AMU shall interface to the CMU via Serial Bus #3. (See Chapter 7 Cabinet Monitor System for Frame Address/ Message Data and Descriptive). The AMU reads the incoming Assembly Address Lines for AMU Serial Bus #3 Frame Address Name (0001 equals AMU Output Assembly 1). A MPU with necessary memory and communications drivers/ receivers (EIA 485) shall be provided. An operating program shall be provided to run the AMU including housekeeping, start up / shut down routines and communications support. The CMU Command Message or Front Panel RESET Switch shall RESET or Clear the AMU

3.8.2 VOLTAGE SENSING

3.8.2.1
The AMU shall sense either the 18 load switch voltage outputs of the SIX PACK Assembly or 36 load switch voltage outputs of the TWELVE PACK Assembly at the field output points. If the output VAC RMS voltage meets or exceeds 25 VAC for 500 ms or longer, the AMU shall set a "Logic 1 " in an associated bit (V1). If the output voltage meets 15 VAC or less or any voltage exists for 200 ms or less, the AMU shall set the associated bit to ""Logic 0" (V1)..

3.8.2.2
The AMU shall sense the same load switch outputs. If the voltage meets or exceeds 70 VAC or greater for 500 ms or more, the AMU shall set a "Logic 1" in an associated bit (V2). If the voltage is 50 VAC or less, or any voltage exists for 200 ms or less, the AMU shall set a "Logic 0" in an associated bit (V2).

3.8.2.3
Voltages and times between the above parameters may or may not set the associate bit to Logic "1". Both positive and negative half wave rectified outputs shall be sensed.

3.8.2.4
All output voltages shall be sensed as true RMS response (up to 3 kHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 3 cycles. If digital means are used in calculating RMS, a minimum of 3 samples shall be taken per positive (between 70 and 110 degrees) and negative (between 250 and 290 degrees) alternation.

3.8.2.5
The AMU shall sense the Flasher Unit Output for the purpose of assurance that the circuit is functioning. Any voltage transition, 0 to 80 VAC (or greater) OR reverse within 1 second duration shall cause an associate bit to be set to Logic "0". No transition during the 1 second period shall cause the associate bit to be set to Logic "1".

3.8.3 CURRENT SENSING

3.8.3.1
The AMU shall sense the output current of the switchbacks and compare each current to two settings (equal or greater). Setting 1 shall be set at 100 mA RMS and Setting 2 at 200 mA. The settings shall be settable from 10 mA to 2 A in 10 mA increments. If the switch pack current meets or exceeds the two settings for over 750 ms, a "logic 1" shall be placed in the associated bits (I1 and I2).

3.8.3.2
The AMU shall current sense the coils of the Flash Transfer Relays for FTR failure .If the current is less than 60 ma for 100 ms, a Logic "1" shall be set in a associate Bit ( ). If the current is 61 ma or greater for 100 ms, the associate bit shall be set at Logic "0".

3.8.3.3
The current sensing toroids shall meet the following requirements:

Linearity	**0 to 10 Amps with voltage range of 85 to 135 VAC.**
Input Impedance	**100 Ohms**
Output	**1.3 mV Signal @ 10 Amps**
Temperature	**-60 to +85 degrees C**
Lead wires	**Micro-Coaxial Type**

3.8.4 POWER REQUIREMENTS

3.8.4.1
The AMU shall generate its own power supply voltage from the incoming VAC using no more than 5 Watts. All generated voltages shall be isolated from the cabinet power supply voltages.

3.8.5 AMU FRONT PANEL

3.8.5.1
A VAC POWER Indicator shall be provided. The indicator shall display ON when the AC+ is 99 +/- 2 VAC or greater and OFF when the voltage is 90 VAC or lower. Between 90 and 99 VAC the indicator shall flash at a 1 Hz rate.

3.8.5.2
A Serial Bus #3 Indicator shall be provided. The indicator shall be ON when the communications between the AMU and CMU is operating properly and OFF when it has ceased for 300 ms or greater.

3.8.5.3
A Monitor Error Indicator shall be provided to be ON when an internal diagnostics error is detected.

3.8.5.4
A recessed RESET Switch shall be provided to reset the AMU MPU.

3.8.6 AMU CONNECTOR

3.8.6.1
The AMU Connector shall be a DIN 4161264 Plug Type. The pin assignments are called out on the DETAIL Section.

CHAPTER 3 SECTION 9

MODEL 216-12 & 216-24 ITS POWER SUPPLY UNITS

3.9.1
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.9.2
Two units, 216-12 and 216-24 shall provide +12 and +24 VDC to the cabinet assemblies. They shall be of ferro-resonant design. They shall have no active components and conform to the following requirements:

3.9.2.1
Input Protection - Two 0.5 ohm, 10-watt wire-wound power resistors with a 0.2 µh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 µf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.9.2.2
Line and load regulation shall meet the two power supply ranges for +24 VDC (23.0 to 26 VDC) and +12 VDC (11.65 to 13.35). This includes ripple noise; from 90 to 135 VAC at 60 Hz. , plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 30 degrees C above ambient.

3.9.2.3
Design Voltage - +24 +/- 0.5 VDC and +12 VDC +/- 0.5 VDC at full load, 30 degrees C, 115 VAC incoming after a 30-minute warm-up period.

3.9.2.4 Full Load Current 5 AMPS each for +24 VDC and +12 VDC, minimum.
3.9.2.5 Ripple Noise - 2 volts peak-to-peak and 500 millivolts RMS at full load.
3.9.2.6 LineVoltage - 90 to 135 VAC.
3.9.2.7 Efficiency - 70% minimum.
3.9.2.8 Circuit capacitors shall be rated for 40 volts minimum.

3.9.3
The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

CHAPTER 3 SECTION 10

MODEL 218 SERIAL INTERFACE UNIT (SIU)

3.10.1 GENERAL

3.10.1.1
Descriptive

The SIU shall function as the cabinet assembly communications and control unit. The SIU shall interface with the ATC Controller Unit through Serial Bus 1 and Serial Bus 2 via the ITS cabinet Modular Bus Assembly. When resident in an input assembly, the SIU via Serial Bus #1 shall collect up to 24 possible detector outputs, (logic "1" or "0"); output 12 detector resets (1 per slot) and communicate via Serial Bus #2 to an internal assembly serial bus interfacing with each device slot. When resident in a SIX PACK Output Assembly, it shall control up to 18 Output Load Switches. When resident in a TWELVE-PACK Output Assembly, it shall control up to 36 output load switches.

3.10.1.2
Power Requirements

The SIU shall receive its power from the cabinet +24 VDC power supply. The SIU shall not require more than 300 ma over the voltage range of 16 to 30 VDC and the power surge shall be limited to a maximum of 1.25 amperes from initial application of DC power. The SIU shall not be damaged by insertion to, or removal from, a powered input or output assemblies.

3.10.1.3
Microprocessor/Controller Unit (FCU)

The SIU Controller Unit shall include a microprocessor/controller unit (FCU) together with all required clocking and support circuitry.

3.10.1.4
Memory

Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware or internal Flash memory.

3.10.1.5
Watchdog
A watchdog circuit shall be provided to scan the SIU FCU every 100 ms. If the FCU don't change state of an output for 1 second the WDT shall reset the FCU. The WDT shall be enabled at NRESET going HIGH and shut down at NRESET/LINESYNC transition to LOWQ.

3.10.1.6
Control Signals
The three control signals, NRESET, POWER DOWN and LINESYNC are sent by the ATC to the SIU. The SIU shall shut down when LINESYNC and NRESET transition to LOW (and stay LOW for 500 ms). When LINESYNC begins to operate and NRESET goes HIGH, the SIU FCU shall reset and begin to operate. The SIU shall reset when the following occurs:

Reset Switch
LINESYNC & NRESET transition HIGH
+5 VDC out of regulation
FCU Watchdog

3.10.1.7
Time Reference
The SIU shall have a 1 KHz Time Reference to provide system response time stamps. The 1KHz Time Reference shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second). A 32-bit Millisecond Counter shall be provided for "time stamping." Each 1 KHz reference interrupt shall increment the Millisecond Counter.

3.10.1.7.1
Millisecond Interrupt
MILLISECOND Interrupt shall be activated by the 1 KHz reference once per millisecond. A timestamp rollover flag set by MC rollover shall be cleared only on command.

3.10.1.7.2
LINESYNC Interrupt
The LINESYNC signal is generated by the controller power supply. LINESYNC Interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ((60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ((500 consecutive ms interrupts).

3.10.1.7.3
Line Frequency Reference

Line Frequency Reference Interrupt shall be generated by both the 0-1 and 1-0 transitions of the Line Frequency Reference signal. The Line Frequency Reference interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ((60 consecutive Line Frequency Reference interrupts). The Line Frequency Reference interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the Line Frequency Reference signal once a second. A Line Frequency Reference error flag shall be set if the Line Frequency Reference interrupt has not successfully executed for 0.5 seconds or longer ((500 consecutive millisecond interrupts). The electrical characteristics of the Line Frequency input are as follows:

3.10.2 INPUTS and OUTPUTS

3.10.2.1
Descriptive

The SIU shall be provided with and control 4 optically coupled inputs, 8 Parallel Inputs, 16 Parallel Outputs, 23 Parallel Input/Outputs, 2 Serial Ports and one serial transfer port.

3.10.2.2
Optically-Coupled Inputs

The 4 Optically coupled inputs are reserved for special functions.
These inputs shall be used for low-true DC applications when the Opto Common pin is connected to the 24- VDC supply.

3.10.2.3
Parallel Inputs

Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

3.10.2.4
Parallel Outputs

Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA

minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 (s when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ± 2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second. Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

3.10.2.4
Parallel Input/Output

Each parallel Input/Output function contains all of the functions listed . These can be used for either Inputs or Outputs, and are intended to be used on input and output assemblies of higher density such as the TWELVE PACK Output Assembly. In this case, the SIU uses the OPTION lines to sense that it resides in a "double-density" output assembly. The software then uses the I/O lines to provide the additional outputs.

3.10.2.5
Function and control

For function and control requirements see Chapters Seven, Section 1 and Nine, Sections Two and Three.

3.10.2.6
Serial Ports

The SIU FCU shall have a minimum of two serial ports. Port 1 shall interface with System Serial Bus 1 providing communications with the 2070 Controller Unit and the SIU. See Chapter 9, Section 3 for Serial Communication Circuitry Requirements and Command/ Response Messages. Also see Chapter 7, Section 1 for SDLC SIU address and additional messages. SIU Port 2 shall be routed to the SIU Front Panel DB 9 Pin Connector providing EIA 232 TXD/RXD lines, asynchronous, 19.2 Kbps interface between FCU and a External Terminal for SIU Status. Software shall be provided to report current Unit Status.

3.10.2.7
Serial Transfer Port

The SIU shall interface with the System Serial Bus #2 (EIA 485 Synchronous Lines) via Standard Receivers /Drivers. The SIU board TTL Logic lines shall be converted to EIA 423 Drivers / Receivers for interface to the input assembly INBUS. TX and

RX are referenced to the SIU. The present INBUS shall be an Asynchronous 19.2 Kbps System using the Assembly four slot address pins. The detector shall have two internal unit switches for the 5th and 6th bits to make up the assembly name. The detector shall receive the ATC Command with the address frame number identifying the detector such as 1CH (Input Assembly 2, Slot 12)). The Detector shall then respond with the appropriate message.

3.10.2.7.1

The SIU shall be provided with INBUS TXC and RXC Drivers / Receivers for a future advanced input assembly with "Smart Devices". The Drivers / Receivers shall be delivered disabled, but with jumper enable capability. This shall allow synchronous high speed communications. The INBUS components shall be rated for 1 Megabps minimum. Each Clock Output to the INBUS shall have three post shunt jumpers.

3.10.2.7.2
The TXD and RXD Lines shall have termination 100 ohm resistors adjacient to Input Assembly Slot 1.

3.10.3 HARDWARE REQUIREMENTS

3.10.3.1
Size and Front Panel Handle

The SIU Module is physically composed of a printed circuit board with a DIN 96-pin connector on the connector end (opposite the front panel). A "U" handle shall be mounted on the front panel for insertion / extraction.

3.10.3.2
Front Panel Indicators, Connector and Reset Switch

Six indicators shall be provided on the front panel, as follows:

SIU Active	**Serial Bus 1 TXD**
SIU Power	**Serial Bus 1 RxD**
INBUS / Serial Bus 2 TXD	**INBUS / Serial Bus 2 RxD**

The Serial Bus 1 Indicators shall be activated by the FCU. Serial Bus 2 / INBUS Indicators shall be sensed and activated at the Logic stage between the 485 and 423 Driver / Receiver signal lines. The SIU Power Indicator shall indicate that the SIU +5 VDC power supply is within regulation. The SIU Active Indicator shall be controlled via SIU WDT Output. The SIU front panel shall provide a recessed RESET Switch. A DB-9S Connector shall be mounted on the front panel for Port 2 Entry. The connector pin assignment is Pin 2- RX Data, Pin 3- TX Data and Pin 5- Signal Ground.

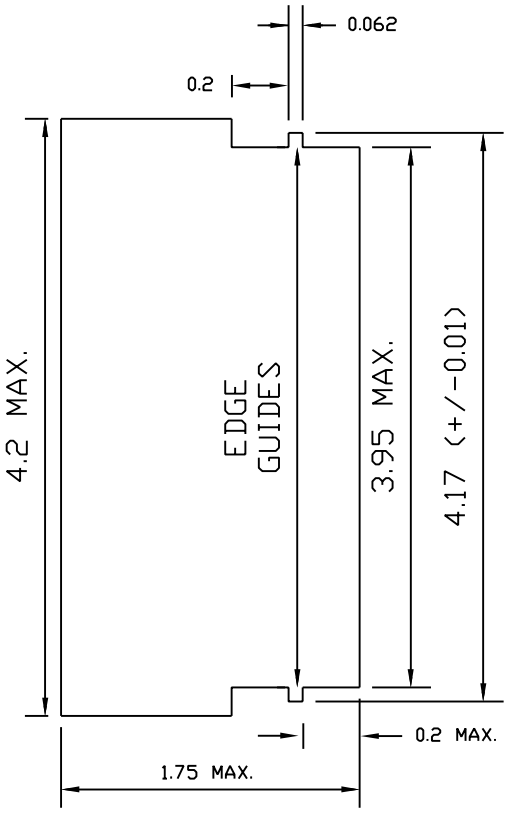
CHAPTER 3 SECTION 11
CHAPTER DETAILS

TABLE OF CONTENTS

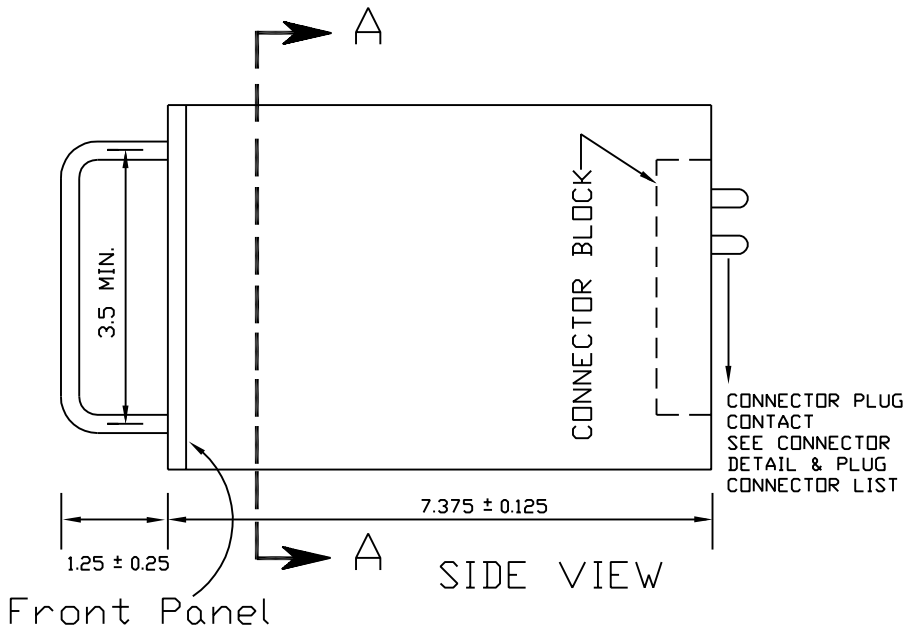
Section Notes:

All measurements shall be in inches.

MODEL 200 SWITCH PACK & 204 FLASHER UNITS



CROSS SECTION A-A



SIDE VIEW

MODEL PLUG CONNECTORS LIST (OR EQUAL)

MODEL 200 - BEAU P-5412-LAB
MODEL 204 - BEAU P-5406-LAB
MODEL 205 - BEAU P-5408-LAB
MODEL 206 - BEAU P-5406-LAB

MODEL 200, 204, 205, 206 CONNECTOR DETAIL

PIN	FUNCTION	PIN	FUNCTION	PIN	Function
1	AC+	7	Load Circuit #1	1	Coil
2	Equip. Ground	8	Load Circuit #2	2	Coil
3	Red Output	9	Equip. Ground	3	NC CKT1
4	Not Assigned	10	AC-	4	NC CKT2
5	Yellow Output	11	AC+	5	Common CKT1
6	Red Input	12	Not Assigned	6	Common CKT2
7	Green Output			7	NO CKT1
8	Yellow Input			8	NO CKT2
9	+24 VDC				
10	Green Input				
11	Not Assigned				
12	Not Assigned				

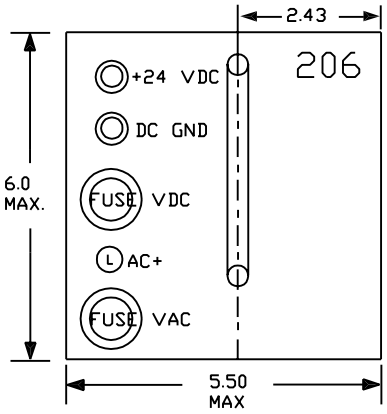
TITLE: MODEL 200 SWITCH PACK & 204 FLASHER UNITS

NO SCALE

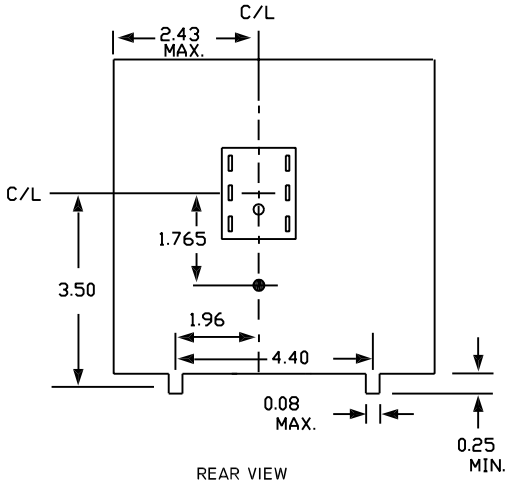
TEES, NOV 19, 1999

3-11-1

MODEL 206 TI70 CABINET POWER SUPPLY UNIT



FRONT VIEW

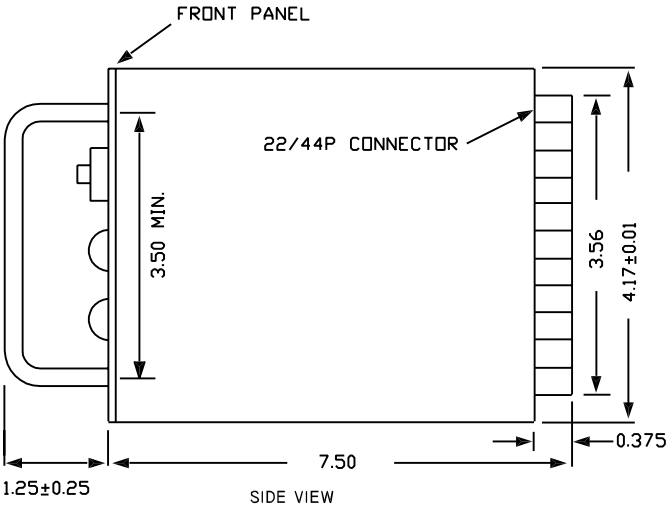


REAR VIEW

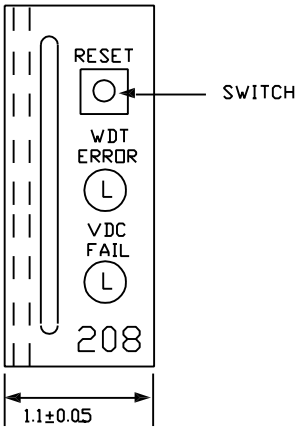
MODEL PLUG CONNECTORS LIST (OR EQUAL)

MODEL 200 - BEAU P-5412-LAB
MODEL 204 - BEAU P-5406-LAB
MODEL 205 - BEAU P-5408-LAB
MODEL 206 - BEAU P-5406-LAB

MODEL 208 TI70 TMU MONITOR UNIT



SIDE VIEW



MODEL 208 MONITOR UNIT PIN ASSIGNMENT

PIN	FUNCTION
1/A	WDT Lamp (External)
2/B	Circ. Common # 1 & # 2
3/C	Normally Closed, Circ. # 1
4/D	AC+
6/F	Normally open, Circ. # 2

PIN	FUNCTION
8/J	AC-
13/P	+24 VDC
18/V	WDT IN
21/Y	WDT Ext. Reset
22/Z	DC Ground

"U" SHAPED ROD HANDLE FABRICATED OF 0.25 +/- 0.05 DIAMETER, ALUMINUM STOCK, WITH 4.0 +/- 0.125 LENGTH, & ROD CENTER TO CENTER, SHALL BE PROVIDED. THE HANDLE SHALL BE VERTICALLY CENTERED. THE DEPTH FROM THER VERTICAL CENTERLINE OF THE HANDLE ROD TO THE MODULE FRONT PANEL SHALL BE 1.25 +/- 0.125

THE POWER SUPPLY UNIT DIMENSION, FROM FRONT PANEL TO CONNECTOR PLUG, SHALL BE 7.375 + 0.000, -0.125

A STANDARD 8-32 METAL STUD RETAINING SCREW SHALL PROVIDE PROPER SECURING OF THE POWER SUPLY WHEN INSTALLED IN THE PDA USING WASHERS AND A WINGNUT. WHEN TORQUED IN THE LOCKING POSITION NO STRESS SHALL BE APPLIED ON THE MATING SOCKET/PLUG CONNECTOR SURFACE. NO MOUNTING OF CHASSIS SUPPORT SCREWS SHALL PROTRUDE BEYOUND THE MATING SURFACE OF THE POWER SUPPLY CONNECTORS.

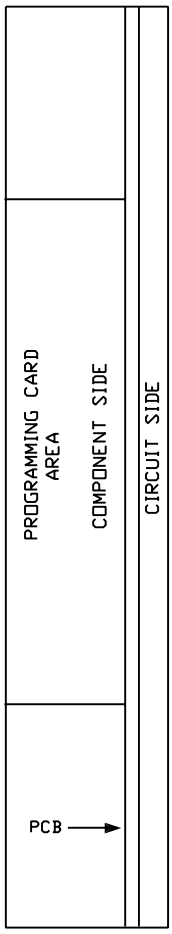
TITLE:
MODEL 206 CABINET POWER SUPPLY & 208 TMU MONITOR UNITS

NO SCALE

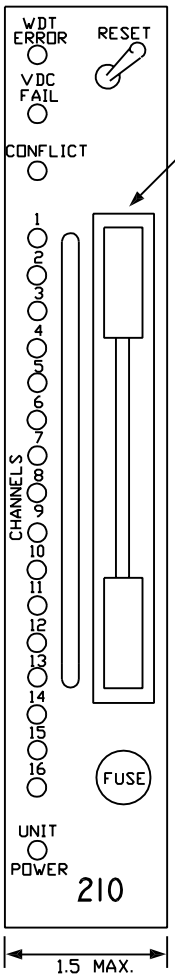
TEES, NOV 19, 1999

3-11-2

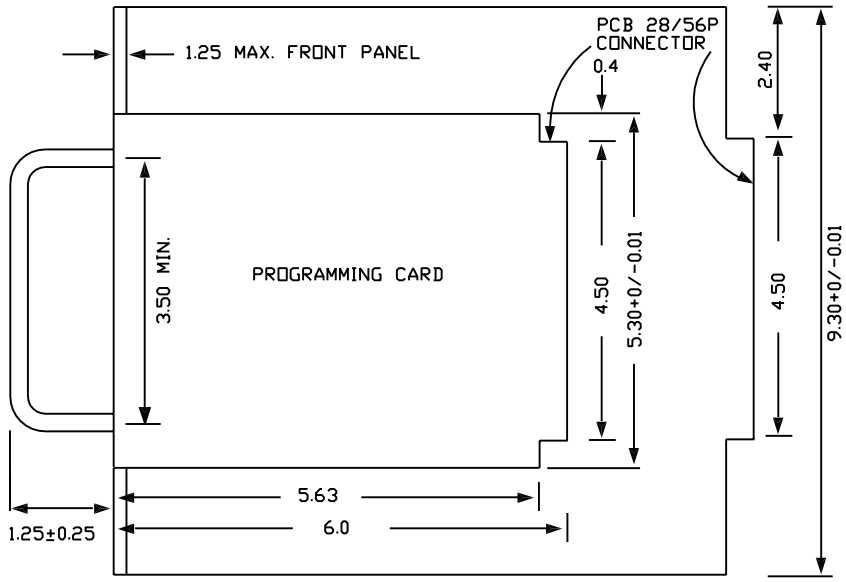
MODEL 210 MONITOR UNIT



REAR VIEW



FRONT VIEW



SIDE VIEW

TITLE: MODEL 210 T170 MONITOR UNIT		
	NO SCALE	
	TEES, NOV 19, 1999	3-11-3

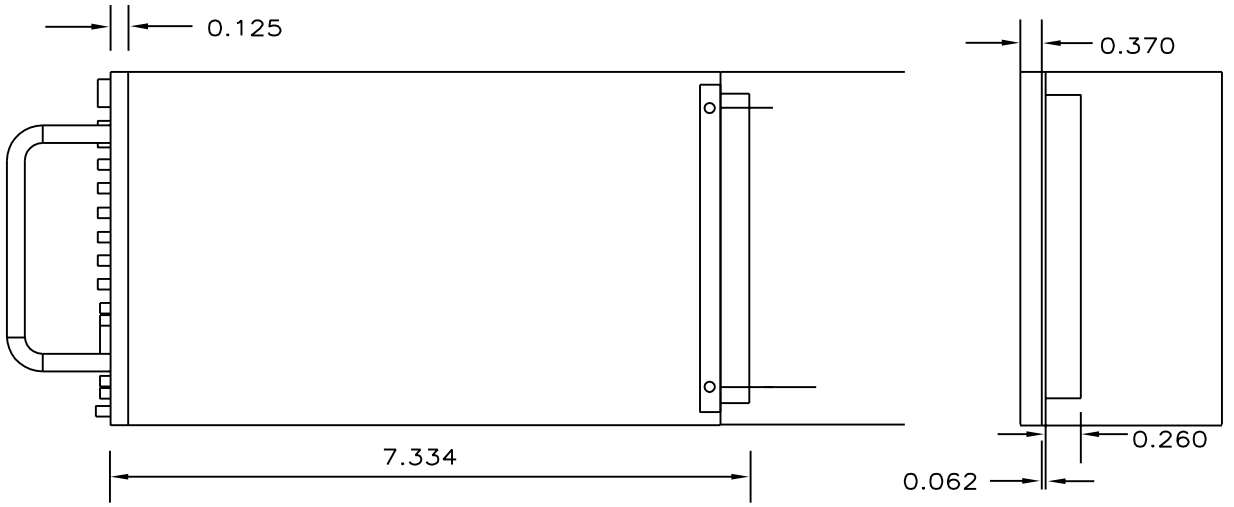
MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC− *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25	BB	Stop Time
25	Tied Together)	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

TITLE: MODEL 210 MONITOR UNIT & PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS		
	NO SCALE	
	TEES, NOV 19, 1999	3−11−4

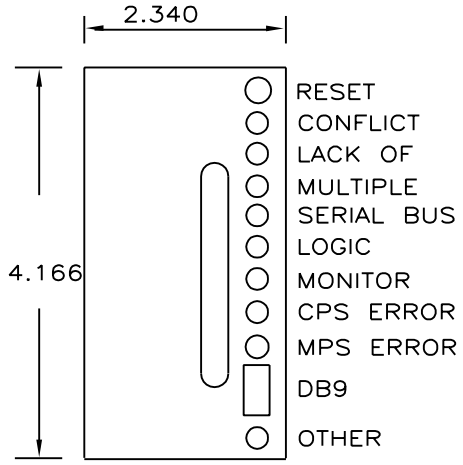


SIDE VIEW

END VIEW

CMU PIN ASSIGNMENTS

Pin #	FUNCTION	Pin #	FUNCTION
A1	+24 VDC in	B1	NA
A2	+12 VDC in	B2	External Reset
A3	VDC Ground	B3	NA
A4	Monitor Interlock	B4	NA
A5	NA	B5	NA
A6	NA	B6	NA
A7	SB1 TxD+	B7	SB1 TxD−
A8	SB1 RxD+	B8	SB1 RxD−
A9	SB1 TxC+	B9	SB1 TxC−
A10	SB1 RxC+	B10	SB1 RxC−
A11	NA	B11	NA
A12	NA	B12	NA
A13	NA	B13	NA
A14	NA	B14	NA
A15	LINE SYNC.+	B15	LINE SYNC.−
A16	N RESET+	B16	N RESET−
A17	PWRDOWN+	B17	PWRDOWN−
A18	SB3 TxD+	B18	SB3 TxD−
A19	SB3 RxD+	B19	SB3 RxD−
A20	SB3 TxC+	B20	SB3 TxC−
A21	LF Status	B21	LF Status
A22	CMU Relay Output	B22	CMU Relay Output
A23	CB Trip Status	B23	CB Trip Status
A24	MC Coil	B24	NA
A25	MC Secondary	B25	NA
A26	FTR Coil	B26	AC+ Main***
A27	Door Switch Front	B27	AC− Main***
A28	Door Switch Rear*	B28	NA
A29	NA	B29	NA
A30	AC+ Filtered**	B30	NA
A31	AC− Filtered**	B31	NA
A32	NA	B32	EQ Ground



FRONT VIEW

* Door Switch Rear (reserved)
** Filtered Power input for use with Signal Monitor Unit power supply.
*** AC+ Main used for monitor act/deact.
Note: SB stands for Serial Bus, LB stands for Load Breaker, MC stands for Mercury Contactor, FTR stands for Flash Transfer Relay.

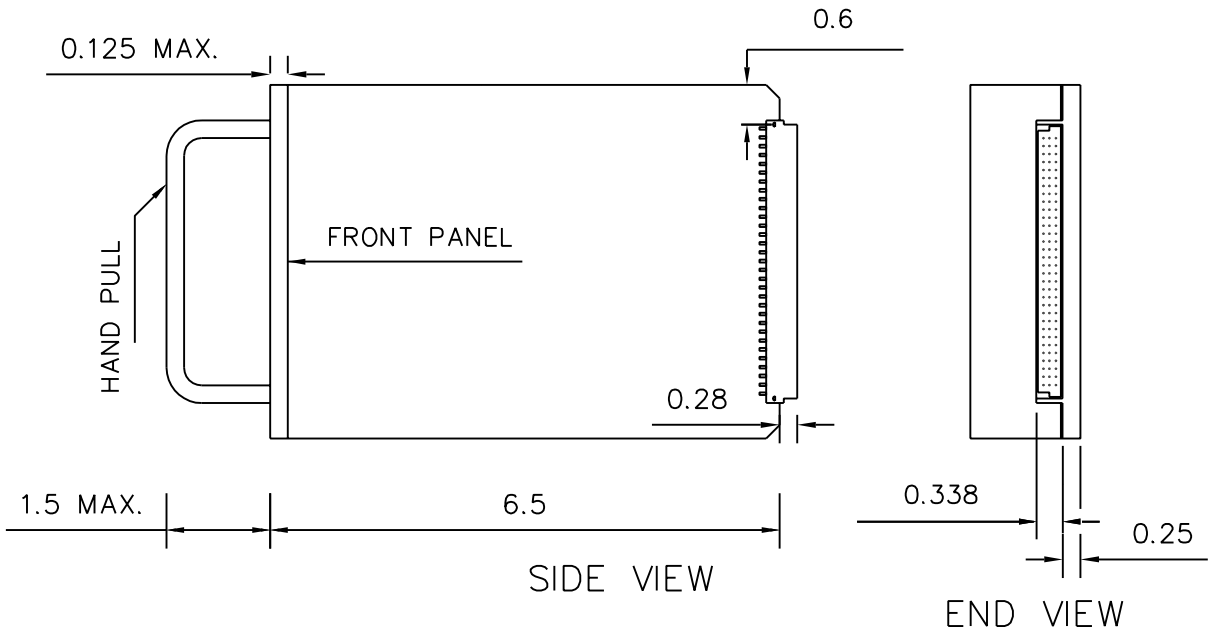
TITLE:

MODEL 212 CMU DETAILS

NO SCALE

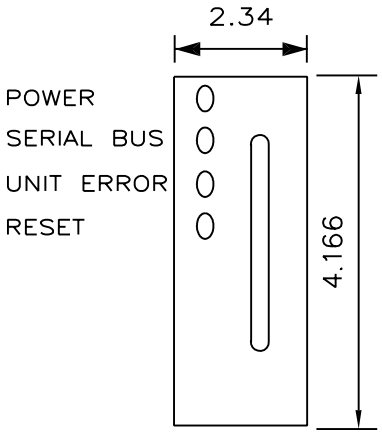
TEES, NOV 19, 1999

3−11−5



AMU PIN ASSIGNMENTS

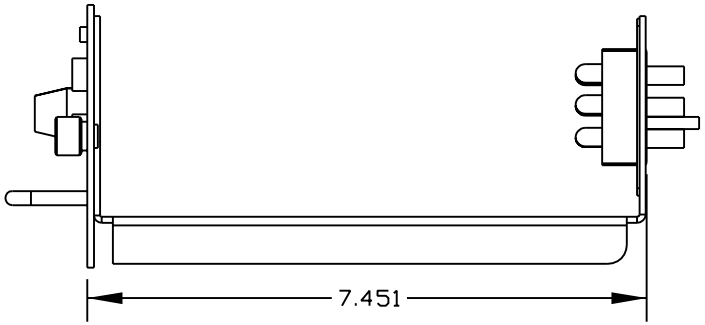
Pin #	FUNCTION	Pin #	FUNCTION
A1	+24 VDC in	B1	ADDR 0
A2	VDC Ground	B2	ADDR 1
A3	NA	B3	ADDR 2
A4	NA	B4	ADDR 3
A5	SB3 TxD+	B5	SB3 TxD−
A6	SB3 RxD+	B6	SB3 RxD−
A7	SB3 TxC+	B7	SB3 TxC−
A8	FTR1 COIL+	B8	FTR1 COIL−
A9	FTR2 COIL+	B9	FTR2 COIL−
A10	FTR3 COIL+	B10	FTR3 COIL−
A11	I Coil1+	B11	I Coil1−
A12	I Coil2+	B12	I Coil2−
A13	I Coil3+	B13	I Coil3−
A14	I Coil4+	B14	I Coil4−
A15	I Coil5+	B15	I Coil5−
A16	I Coil6+	B16	I Coil6−
A17	NA	B17	NA
A18	Switchpack 1 Red	B18	Switchpack 2 Red
A19	Switchpack 1 Yellow	B19	Switchpack 2 Yellow
A20	Switchpack 1 Green	B20	Switchpack 2 Green
A21	Switchpack 3 Red	B21	Switchpack 4 Red
A22	Switchpack 3 Yellow	B22	Switchpack 4 Yellow
A23	Switchpack 3 Green	B23	Switchpack 4 Green
A24	Switchpack 5 Red	B24	Switchpack 6 Red
A25	Switchpack 5 Yellow	B25	Switchpack 6 Yellow
A26	Switchpack 5 Green	B26	Switchpack 6 Green
A27	AC+ Main	B27	AC− Main
A28	NA	B28	NA
A29	NA	B29	EQ Ground
A30	NA	B30	NA
A31	FL1 CKT 1	B31	FL2 CKT 1
A32	FL1 CKT 2	B32	FL2 CKT 2



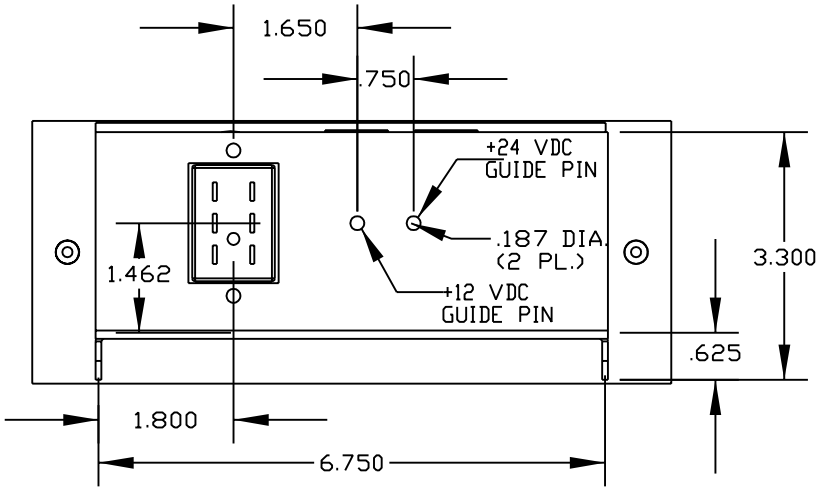
TITLE:

MODEL 214 AMU DETAILS

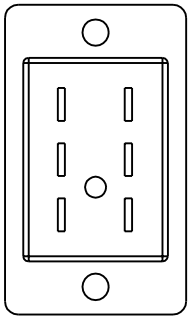
	NO SCALE	
	TEES, NOV 19, 1999	3−11−6



SIDE VIEW

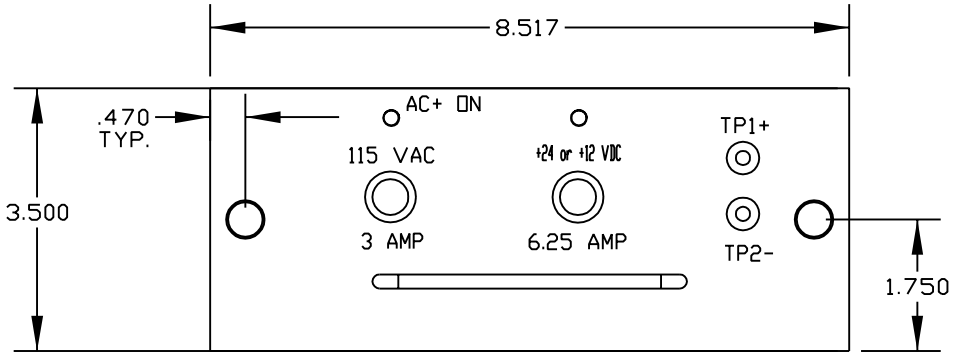


REAR VIEW



SOCKET FRONT VIEW

7	+24 VDC	8	+12 VDC
9	DC GROUND	10	EQ GROUND
11	AC-	12	AC+



FRONT VIEW

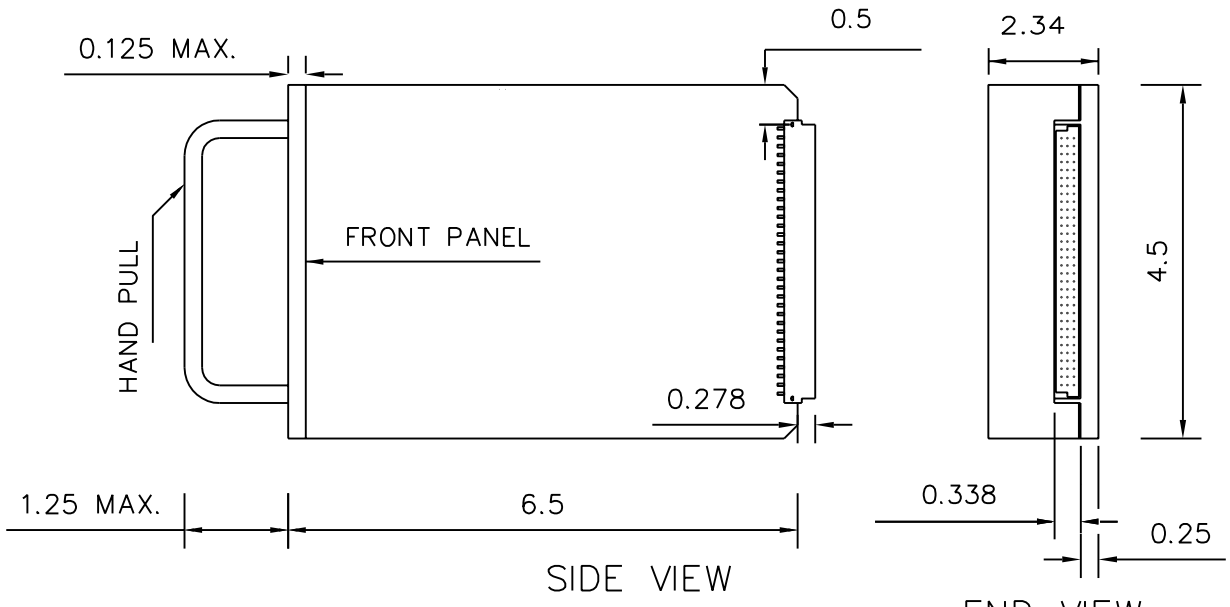
TITLE:

MODEL 216 ITS CABINET
POWER SUPPLY UNIT

NO SCALE

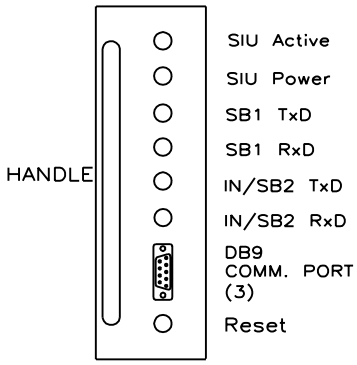
TEES, NOV 19, 1999

3-11-7



SIU PIN ASSIGNMENTS

PIN	SIU ROW A	SIU ROW B	SIU ROW C
1	+24 VDC in	+24 VDC in	+24 VDC in
2	Output 1	Output 2	N.C.
3	Output 3	Output 4	SB1 TxD +
4	Output 5	Output 6	SB1 TxD –
5	Output 7	Output 8	SB1 RxD +
6	Output 9	Output 10	SB1 RxD –
7	Output 11	Output 12	SB1 TxC +
8	Output 13	Output 14	SB1 TxC –
9	Output 15	Output 16	SB1 RxC +
10	Output17/Input25	Output18/Input26	SB1 RxC –
11	Output19/Input27	Output20/Input28	LINE SYNC. +
12	Output21/Input29	Output22/Input30	LINE SYNC. –
13	Output23/Input31	Input 1	N RESET +
14	Input 2	Input 3	N RESET –
15	Input 4	Input 5	PWRDOWN +
16	Input 6	Input 7	PWRDOWN –
17	Input 8	Input9/Output25	SB2 TxD +
18	Input10/Output26	Input11/Output27	SB2 TxD –
19	Input12/Output28	Input13/Output29	SB2 RxD +
20	Input14/Output30	Input15/Output31	SB2 RxD –
21	Input16/Output32	Input17/Output33	SB2 TxC +
22	Input18/Output34	Input19/Output35	SB2 TxC –
23	Input20/Output36	Input21/Output37	SB2 RxC +
24	Input22/Output38	Input23/Output39	SB2 RxC –
25	Input24/Output40	Opto Input 1 (*)	INBUS TxC
26	Opto Input 2 (*)	Opto Input 3 (*)	INBUS RxC
27	Opto Input 4 (*)	Opto Input Ground	Option – 0
28	Address–0	Address–1	Option – 1
29	Address–2	Address–3	Option – 2
30	INBUS TxD	INBUS RxD	Option – 3
31	Equipment Ground	AC Line Reference	Equipment Ground
32	24 VDC Ground	24 VDC Ground	24 VDC Ground



FRONT VIEW

TITLE:

MODEL 218 SIU DETAILS

	NO SCALE	
	TEES, NOV 19, 1999	3–11–8

CHAPTER 5

SPECIFICATION FOR DETECTOR SENSOR UNITS, ELEMENTS AND ISOLATORS

MODEL 222E TWO-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 224E FOUR-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 231E MAGNETIC DETECTOR SENSING ELEMENT

MODEL 232E MAGNETIC DETECTOR SENSOR UNIT

MODEL 242 TW0-CHANNEL DC ISOLATOR

MODEL 252 TWO-CHANNEL AC ISOLATOR

TABLE OF CONTENTS

CHAPTER 5 SECTION 1

GENERAL REQUIREMENTS

5.1.1
The sensor and isolator channels shall be operationally independent from each other. Each sensor or isolator channel shall draw no more than 50 mA from the +24 VDC cabinet power supply and shall be insensitive to 700 millivolts RMS ripple on the incoming +24 VDC line.

5.1.2
The sensor unit or isolator front panel shall be provided with the following:

Hand pull to facilitate insertion and removal from the input.
Control switches.
Channel visual indication of detection or incoming signal.

5.1.3
Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs.

5.1.4
A valid sensor channel input shall cause a channel Ground True Output to the controller unit. of a minimum 100 ms in duration. An onboard two-post shunt jumper shall be provided to disallow this requirement when the jumper is in a OPEN position.

5.1.5
The sensor unit or sensing element shall operate and interface successfully with an associate CALTRANS Standard Sensing Unit or Element.

5.1.6
The output transistor shall switch from OFF to ON state or ON to OFF state in 20 µs or less.

5.1.7
Each Enhanced (E) Sensor Unit shall provide a Tri State EIA 423 Serial Port for interface with through pins 19 and 21 of the unit connector to the assembly SIU Connector C03. Each sensor unit shall read in the Slot Address pins located at unit connector for unit slot Identification. Four onboard switches shall match the upper 5th to 8th bits associated Assembly name. Slot Pin 22 shall turn on the SIU Drivers allowing RXD to the ATC. Status and report messages shall meet SDLC Protocol transmitting at 19,200 bps. Said Messages shall be as called out by the user.

5.1.8
Onboard protection shall be provided to enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 1000 Volts directly across the input pins with no load present. With a dummy load of 5 Ohms, protection shall enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 2000 Volts directly across either the input pins or from either side to equipment ground.

CHAPTER 5 SECTION 2

MODEL 222E & 224E LOOP DETECTOR SENSOR UNIT REQUIREMENTS

5.2.1
The sensor unit channel shall produce an output signal when a vehicle passes or remains over loop wires embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit.

5.2.2
An open, shorted or otherwise malfunctioning loop shall cause the sensor unit channel to output a constant signal state. A two post shunt jumper or approved switch shall be provided to dictate output state upon malfunction. The jumper in closed position (Ground True) shall cause a Ground True Output to the controller unit. An open position (Ground False) shall cause a Ground False Output to the controller unit. An indicator labeled "EOS" (Event Output Status) shall be provided on the front panel. When in closed position, the indicator shall be ON. A second indicator per channel labeled "EVENT" shall be provided indicating a malfunctioning loop or tracking condition. The indicators shall be reset by the Unit RESET Switch.

5.2.3
Each sensor unit channel shall be capable of detecting all types of AGENCY licensed motor vehicles when connected to the loop configuration/lead-in requirements of Heading 5.2.9.1.

5.2.4
The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 µH with a Q-parameter as low as 5 at the sensor unit operating frequency.

5.2.5
Loop inputs to each channel shall be transformer isolated.

5.2.6
Each individual channel shall have a minimum of 4 switch selectable operating frequencies.

5.2.7
The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes or changes in applied power shall not cause an actuation.

5.2.8
Each sensor unit channel shall have PULSE and PRESENCE selectable modes.

5.2.8.1
In the PULSE MODE, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (+/- 25) ms in duration. Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically "tune out" the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be 3 seconds maximum.

5.2.8.2
In the PRESENCE MODE, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence. The channel sensitivity settings 2 & 6 shall provide presence detection of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

	MINIMUM TIME DURATION IN MINUTES	DETECTOR INPUT INDUCTANCE CHANGE
SETTING 6	3 10	0.02% or more 0.06% or more
SETTING 2	4	1.00% or more

5.2.9
Sensitivity

5.2.9.1
California Standard Plan ES-5A & B Loop Configurations. (California Department of Transportation Standard Plans.)

5.2.9.1.1
Single Type A, B, Q or Round Loop with a 250 foot lead-in cable.

5.2.9.1.2
Single Type A, B, Q or Round Loop with a 1000 foot lead-in cable.

5.2.9.1.3
4 Type A, B, or Q Loops connected in series/parallel with a 250 foot lead-in cable.

5.2.9.1.4
4 Type A, B, Q or Round Loops connected in series with a 1000 foot lead-in cable.

5.2.9.1.5
One 50 foot Type C Loop with a 250 foot lead-in cable.

5.2.9.2
Each sensor unit channel shall be equipped with 7 selectable (digitally read) sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification:

SETTING	SESITIVITY	SETTING	SENSITIVITY
1	0.64 % delta L	5	0.04 % delta L
2	0.32 % delta L	6	0.02 % delta L
3	0.16 % delta L	7	0.01 % delta L
4	0.08 % delta L	0	Channel OFF

5.2.9.2.1
All sensitivity settings shall not differ +/- 40% from the nominal value chosen.

5.2.9.3
Each sensor unit channel shall not detect vehicles, moving or stopped, at distances of 3 feet or more from any loop perimeter, in all configurations listed in paragraph 5.2.9.1.

5.2.10
Response time of the sensor unit channel for Sensitivity Settings 1, 2 & 3 shall be less than 5 +/- 1 ms at an approximate loop frequency of 40 KHZ. That is, for any decreased inductive change which exceeds its sensitivity threshold, the channel shall output a ground true logic level within 5 +/- 1 ms. When such change is removed, the output shall become an open circuit within 5 +/- 1 ms.

5.2.11
The sensor unit channels shall begin normal operation within 2 seconds after the application of power or after a reset signal of 30 µs.

5.2.12
Tracking Rate – The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.13
Tracking Range - The sensor unit shall be capable of normal operation as the input inductance is changed from +/- 5.0% from the quiescent tuning point regardless of internal circuit drift. The sensor unit shall be capable of normal operation as the input resistance is changed from +/- 0.5% from the quiescent tuning point regardless of internal circuit drift.

5.2.14
Temperature Change – The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1 degree C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18 degrees C between the inside and outside air shall not affect the proper operation of the sensor unit.

CHAPTER 5 SECTION 3

MAGNETIC DETECTOR REQUIREMENTS

5.3.1 MODEL 231E MAGNETIC DETECTOR SENSING ELEMENT

5.3.1.1
Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 57 mm maximum in diameter, have no sharp edges, and its length not to exceed 450 mm (18 in). The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a minimum 1.27M lead-in cable. Leakage resistance shall be a minimum of 10 megohms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 20 degrees (+/- 3 degrees) C. The salt water bath concentrate shall be one fourth ounce of salt per gallon of water.

5.3.1.2
Each sensing element including lead-in shall have a DC resistance of less than 3500 ohms and an inductance of 20 Henrys +/- 15 %.

5.3.2 MODEL 232E TWO CHANNEL MAGNETIC DETECTOR SENSING UNIT

5.3.2.1
When resident in a active cabinet input assembly and attached to one or more Model 231E Sensing Elements resident in conduit under the travelway, the sensing channel shall output a Ground True Output to the Controller Unit when sensing an induced voltage caused by a California Licensed Vehicle passing within 1.83 M from an element with a 305 M of lead-in cable at all speeds between 5 and 130 KMPH. The sensing channel output shall be continuous as long as the vehicle is detected. A digital reading switch with 8 selected step positions for Gain (O to Full) and a momentary test switch providing a voltage test input shall be furnished for each channel on the front panel.

CHAPTER 5 SECTION 4

MODEL 242 TWO-CHANNEL DC ISOLATOR REQUIREMENTS

5.4.1
The Model 242 DC Isolator Channel shall provide isolation between a VDC input circuit (external electrical switch closure) and the controller unit input. The minimum isolation shall be 1000 Megohms and 2,500 VDC measured between the input and the output of the same channel.

5.4.2
Each isolation channel shall have a front panel mounted test switch to simulate valid input. The test switch shall be a single-pole double-throw, three position CONTROL test switch: The position assignment shall be UP – constant ON; MIDDLE – OFF; and DOWN – momentary ON.

5.4.3
The isolator shall have an internal power supply supplying 20 +/- 4 VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet power supply.

5.4.4
A channel contact closure input of 2 ms or less shall not cause an output (ground true) to the controller. An input of 7 ms or greater shall cause an output to the controller. An input of duration between 2 and 7 ms may or may not cause an output to the controller. .

5.4.5
Each isolation channel field input shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA nor more than 40 mA to an electrical contact closure or short from the power supply.

CHAPTER 5 SECTION 5

MODEL 252 TWO-CHANNEL AC ISOLATOR

5.5.1
The Model 252 Two-Channel AC Isolator shall contain 2 isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design which provides reliable operation.

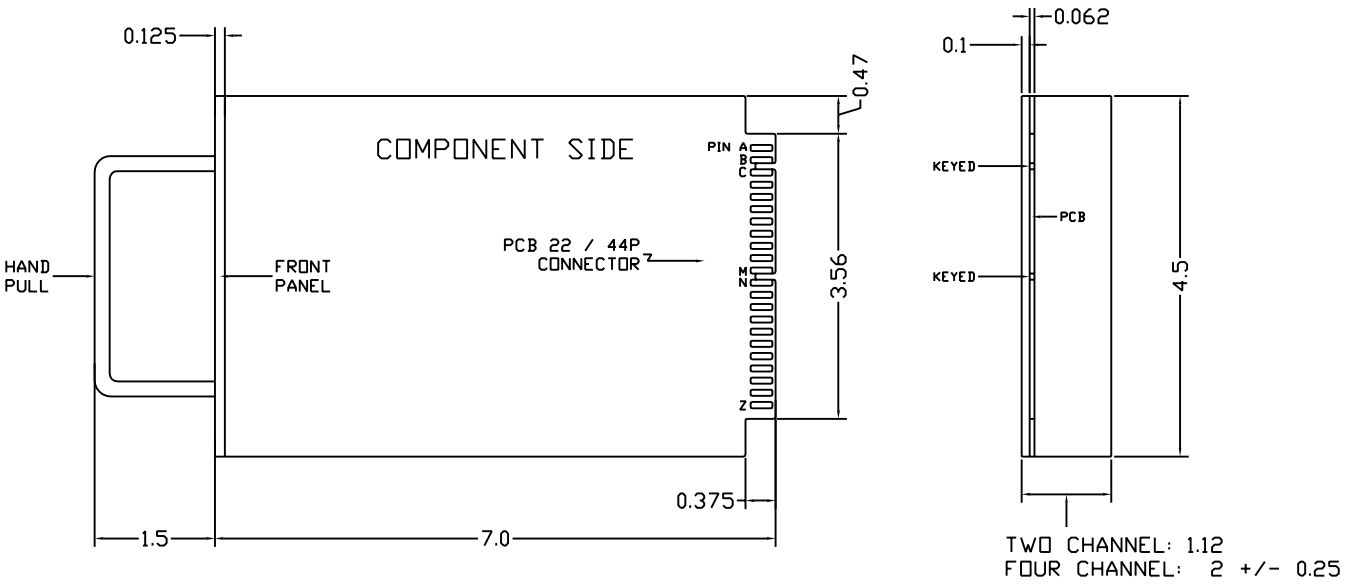
5.5.2
A channel input voltage "Von" of 80 +/- 5 VAC applied for a minimum duration of 100 ms shall cause an output (Ground True) to the controller unit.

5.5.3
A channel input voltage "Voff" (Von minus 10 VAC) applied for a minimum duration of 100 ms shall cause an output (Ground False) to the controller unit.

5.5.4
A two post jumper shall be provided to select inverted output states for Von and Voff. When in CLOSED position (Grounded) Von shall cause a Ground False output. An indicator shall be provided on the front panel labeled 'RR" which shall indicate a Voff input, Ground True output.

5.5.5
The input impedance of each channel shall be between 6,000 - 15,000 Ohms at 60 Hz.

5.5.6
The minimum isolation shall be 1000 Megohms between the input and output terminals at 500 AC applied voltage.



SIDE VIEW

END VIEW

CONNECTOR ASSIGNMENTS

ISOLATORS	SENSORS	PIN		ISOLATORS / SENSORS
DC GROUND		A	1	N/A
+24 VDC		B	2	N/A
N/A	EXT RESET	C	3	SLOT ADDRESS 3
INPUT #1		D	4	INPUT #1
INPUT #1		E	5	INPUT #1
OUTPUT #1 (C)		F	6	SLOT ADDRESS 0
OUTPUT #1 (E)		H	7	N/A
INPUT #2		J	8	INPUT #2
INPUT #2		K	9	INPUT #2
EQUIPMENT GROUND		L	10	SLOT ADDRESS 1
AC-		M	11	AC-
AC+		N	12	AC+
N/A	INPUT #3	P	13	INPUT #3
N/A	INPUT #3	R	14	INPUT #3
N/A	OUTPUT #3 (C)	S	15	SLOT ADDRESS 2
N/A	OUTPUT #3 (E)	T	16	N/A
N/A	INPUT #4	U	17	INPUT #4
N/A	INPUT #4	V	18	INPUT #4
OUTPUT #2 (C)		W	19	EIA 423 TX DATA
OUTPUT #2 (E)		X	20	N/A
N/A	OUTPUT #4 (C)	Y	21	EIA 423 RX DATA
N/A	OUTPUT #4 (E)	Z	22	COMM. STATUS

NOTES:
1. DIMENSIONS SHALL BE IN INCHES.
2. TOLERANCE DIMENSIONS ARE +/-0.02'' EXCEPT AS NOTED.
3. "U" SHAPE ROD HANDLE SHALL BE FABRICATED OF 0.18'' TO 0.26'' DIAMETER STOCK.

TITLE:

SENSOR UNIT AND ISOLATOR DETAILS

NO SCALE

TEES, NOV 19, 1999

5-6-1

CHAPTER 7

SPECIFICATION FOR CABINET ASSEMBLY

TABLE OF CONTENTS

CHAPTER 7 - SECTION 1

CABINET SYSTEM REQUIREMENTS

7.1.1 GENERAL

7.1.1.1
The Intelligent Transportation System (ITS) Serial Interconnected Cabinet Family is a group of cabinets designed to fulfill a variety of applications (26 have been identified). This specification describes the functional and physical requirements of said cabinets.

7.1.1.2
There are common parts to all cabinets such as Housing, Cage(s), Modular Bus and Power Assemblies, Electronic Communications Terminal Assembly (ECTA), Cabinet Emergency Override System, harnesses and Advanced Transportation Controller (ATC). The Power Distribution Assembly (PDA 5 & 6), Input and Output Assemblies used and their plug in Units shall depend upon application need.

7.1.1.3
The ATC Controller here in referred to shall be the Model 2070 Controller Unit. It is serially connected to the Cabinet via its two serial synchronous ports located at C12 Connector. These two communication links use EIA-485 Drivers/Receivers and Synchronous Data Link Control (SDLC) Protocol to interface with Serial Bus #1 and #2.

7 .1.1.3.1
SERIAL BUS #1 functions as Command/Response for cabinet real-time control and communications. The Serial Bus #1 in concert with the Assembly Model 218 Serial Interface Units (SIU) and the Cabinet Emergency Monitor Unit form physical bus structure.

7.1.1.3.2
The SERIAL BUS #2 functions as Command / Response between the ATC; and the input devices. At present this shall be serially connected between the detectors in the input assemblies and the ATC. In the future assemblies this shall be ATC and System "Smart Devices".

7.1.1.3.3
The CABINET EMERGENCY OVERRIDE SYSTEM senses and monitors load outputs, various operational functions and the bus controls/ communications. It then controls cabinet emergency actions and/or reports to the ATC. The Cabinet Monitoring System is part of the Emergency Override System.

7.1.1.4
The EXTERNAL COMMUNICATIONS TERMINATION ASSEMBLY (ECTA) has been added to provide isolation and linkage to the ATC. It is structured for dual line fiber optics and 8 pairs of communication wires.

7.1.2 CABINET MODEL NUMBER AND CONSISTENCY

7.2.1

The ITS Cabinets shall consist of a package of items needed to carry out the specific Application. The Cabinet Package List is:

Cabinet Traffic Signal Application - Series 340

340 - 4 Door Cabinet with "P" Base Ground Mount
342 – 2 Door Cabinet with "170" base Ground Mount
346 - 2 Door Cabinet with" 170" base, Adaptor Mount

Cabinet Traffic Management Application - Series 350

354 – 2 Door Cabinet with "170" base Ground Mount for Ramp Metering & ETC.
356 – 2 Door Cabinet with "170" bas, Adaptor mount.

Package Items	340	342	346	354	356
Housing #1/Cage #1	-	1	-	1	-
Housing #2/Cage#2	-	-	1	-	1
Housing#3/ Two Cage#1	1	-	-	-	-
Input Panel	1	1	-	1	1
AC Protected Power Assembly	1	-	-	-	-
AC Filtered Power Assembly #1	2	1	-	1	-
AC Filtered Power Assembly #2	-	-	1	-	1
DC Power/COMM Assembly #1	2	1	-	1	-
DC Power/COMM Assembly #2	-	-	1	-	1
Cage Drawer Assembly	1	1	-	1	-
Input Assembly	3	2	1	1	1
Six Pack Output Assembly	1	-	-	1	1
Twelve Pack Output Assembly	1	1	1	-	-
PDA#5 Assembly	1	1	1	-	-
PDA #6 Assembly	-	-	-	1	1
E CT Assembly	1	1	1	1	1
Control/Serial Bus Harness	8	6	4	4	4
Serial Bus 3 Harness	3	1	1	1	1

7.1.3 SERIAL BUS # 1 SYSTEM

7.1.3.1

Serial Bus #1, as noted above, functions as the real-time cabinet control and communications. The Bus Commands are generated in the ATC Controller Unit. They are passed to the assembly Model 218 SIU Units and Model 212 CMU Monitor Unit using EIA 485 COMM/SDLC Protocol Frame Address/Message Packets. The Units read the Four line

Assembly Molex Connector for Assembly Address Number and compares it to the SDLC Address Frame.

7.1.3.2
The following Address Frame numbers are assigned to the assemblies and monitor as:

Output Assembly #1	**01**	**0000 0001**
Output Assembly #2	**02**	**0000 0010**
Output Assembly #3	**03**	**0000 0011**
Output Assembly #4	**04**	**0000 0100**
Input Assembly #1	**09**	**0000 1001**
Input Assembly #2	**10**	**0000 1010**
Input Assembly #3	**11**	**0000 1011**
Input Assembly #4	**12**	**0000 1100**
Input Assembly #5	**13**	**0000 1101**
Cab Monitor Unit	**15**	**0000 1111**

If the Command Address Frame matches the Unit, the Unit reads in the message for processing and response. The Message First Byte is the message name. The Unit responses by setting the SDLC Address Frame to "19" or CPU of the ATC. The Unit sets the Response Packet First Byte to Command Message plus 127 and the appropriate data. The Command / Response required Buffers, Drivers and Messages s are listed in Chapter Nine, Sections two and three. Also note Unit requirements in Chapter 3, Sections 7, 8 and 10 plus the following:

7.1.3.3
Message 61 - ATC COMMUNICATION COMMAND

BYTE	msb							lsb	FUNCTION
1	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**Message 61**
2	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Number of Bytes**
3	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Seconds-Digit 1 ASCI**
4	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Seconds-Digit 2 ASCI**
5	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Minutes-Digit 1 ASCI**
6	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Minutes-Digit 2 ASCI**
7	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Hours -Digit 1 ASCI**
8	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Time Hours -Digit 2 ASCI**
9	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Day of Year -Digit 1 ASCI**
10	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Day of Year -Digit 2 ASCI**
11	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Day of Year -Digit 3 ASCI**
12	**0**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #1 SP 1 & 2**
13	**0**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #1 SP 3 & 4**
14	**0**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #1 SP 5 & 6**
15	**1**	**0**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #2 SP 1 & 2**
16	**1**	**0**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #2 SP 3 & 4**

17	**1**	**0**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #2 SP 5 & 6**
18	**1**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #3 SP 1 & 2**
19	**1**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #3 SP 3 & 4**
20	**1**	**1**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #3 SP 5 & 6**
21	**0**	**0**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #4 SP 1 & 2**
22	**0**	**0**	**g**	**y**	**r**	**g**	**y**	**r**	**Output Assembly #4 SP 3 & 4**
23	**0**	**0**	**g**	**x**	**r**	**g**	**y**	**r**	**Output Assembly #4 SP 5 & 6**

The ATC sends this message to the Monitor for information only. It is used as a comparison to the Assembly Outputs and Report Time Stamping.

SP	**Switch Pack**	**g**	**green Indication**
y	**yellow indication**	**r**	**red Indication**

Message 189 ATC COMMUNICATIONS RESPONSE

BYTE	msb							lsb	FUNCTION
1	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**Message Number**
2	**A**	**B**	**C**	**D**	**E**	**G**	**H**	**F**	**FAULT STATUS 1**
3	**J**	**K**	**L**	**M**	**N**	**P**	**R**	**S**	**FAULT STATUS 2**
4	**T**	**Y**	**Z**	**x**	**x**	**x**	**x**	**x**	**FAULT STATUS 3**

F – LFSA (FLASH or BLANK State)
A – Caused by Cabinet Power Supplies
B – Caused by Serial Bus Error
C – Caused by Channel Conflict
D - Caused by ATC Message 62
E - Caused by Monitor Error
G – Caused by Door Closed and Monitor Unit out
H - Caused by Individual FTR Coil Failed
J– Caused by Transfer Relay Yellow or Red Flash with Normal Output
K - Caused by Logic Signal Error
L – Caused by Lack of indication G, Y or R
M – Caused by Multiple Indication
N - Caused by Circuit Breakers and Mercury Contact Status
P - Caused by Police AUTO/FLASH Switch
R - Caused by PDA Flash Switch
S - Caused by AC line level sense
T - Caused by ATC 2 Second Lack of Communication
Y – Caused by Short Yellow
Z – Caused by Long Yellow
x – Future

7.1.3.4
Message 62 – SET/RESET REPORT COMMAND

BYTE	msb							lsb	FUNCTION
1	0	0	1	1	1	1	1	0	Message Number
2	S	R	O	x	x	x	x	x	Set LFSA or Request Reports
3	Type of Report								

S = 1 will set FLSA as long as SIU Comm Bad The S Transition to 1 the first time and if no report requested shall get the following Message 190 Response. If Report is requested and S set or not Message 190 shall be in Report form called out in Chapter 3, Section 7.

Message 190 – SET/RESET REPORT RESPONSE

BYTE	msb							lsb	FUNCTION
1	1	0	1	1	1	1	1	0	message Number
2	same as message 189								
3	same as message 189								

S - Set Monitor to LFSA R Report Request

7.1.3.5
Message 63 - VARIBLE INPUT COMMAND

BYTE	msb							lsb	FUNCTION
1	0	0	1	1	8	1	1	1	

Message 191 VARIABLE INPUT RESPONSE

BYTE	msb							lsb	FUNCTION
1	1	0	1	1	1	1	1	1	Message Number
2	0	0	0	0	x	x	x	x	Byte count- up to 15 Bytes
3 to 17	x	x	x	x	x	x	x	x	Data - 15 Bytes
18	x	x	x	x	x	x	x	x	Timestamp MSB
19	x	x	x	x	x	x	x	x	Timestamp NMSB
20	x	x	x	x	x	x	x	x	Timestamp NLSB
21	x	x	x	x	x	x	x	x	Timestamp LSB

7.1.3.6
Message 64 VARIBLE OUTPUT COMMAND / RESPONSE

Message 64 Command shall match Message 55 Command except for Byte 2 which denotes the number of output bytes following. Message 191 Response and Message 183 match except for name.

7.1.4 SERIAL BUS #2 SYSTEM

7.1.4.1
Serial Bus #2 as noted is dedicated to gathering preprocessed data from the Cabinet Enhanced Detectors resident in the input assemblies. This serial bus shall be off- line use in operation with the ATC controlling data collection. The Serial Bus #2 is designed to operate Synchronous or Asynchronous 485 lines at selected bps up to 1 Mega-BPS. At Present, it shall be delivered operating at 19,000 bps Asynchronous. The Model 218 SIU shall change 485 to / from Standard 423 used by the INBUS. Each input assembly slot Pin 19 – TXD and Pin 21-RXD shall be INBUS Network for ATC and Detector data request and response.

7.1.4.2
The ATC Message shall use SDLC Format. The Enhanced Detectors shall read two ID addresses for detector name. The four line/ Slot Pin Address, Pins 3,6,10 and 15, shall be use to match name of the detector slot such as "1100" or "12". Four internal detector switches shall be used to ID the assembly address such as "9' equals Input Assembly "#1". The name of the detector in ATC Address Frame shall read "10011100". The Detector shall monitor a ATC Transmission scanning all ATC Outputs. If the Address and Message match up, the detector shall first issue a Ground True Communications Status (Slot Pin 22) to the Assembly SIU at Pin C03. This shall activate INPUT / Serial Bus #2 RXD Drivers. If Status not ground True, the drivers shall be inactive. The response messages inclusive of SDLC frames shall be no more than Twenty bytes. RXD and TXD Lines shall be terminated in the input assembly motherboard adjacent to Slot 1 with 100 Ohm resistor.

7.1.4.3
The next generation input assembly is planned to use DIN 64 or 96 Pin Connectors allowing a better non legacy addressing scheme for "Smart Devices". " Smart Devices" are defined as Advanced Detector and Output Units capable of direct serial communications with the ATC Controller Unit. Synchronous serial port 3 of the ATC CPU is assigned to the Bus and functions as COMMAND linkage to the system.

7.1.4.4
Typical Command/Response Messages shall use the same message format as Serial Bus #1 collecting Operational Status. Detection Speed reports, Occupancy reports, Counts and ETC.

7.1.5 CABINET EMERGENCY OVERRIDE SYSTEM (CEOS)

7.1.5.1
SYSTEM DESCRIPTION

The Emergency System is composed of the Police Panel Switches, Door Switches, Cabinet Power Distribution Assembly with resident Cabinet Monitor Unit, Serial Bus #1, AC Modular Assembly and cable/s, and the Output Assemblies with Flash Transfer Relays and Flash Programmable Matrix Connectors. The purpose of this system is to transfer control from the ATC to the EMERGENCY OVERRIDE SYSTEM Control when called for by the

Cabinet Monitoring System or Manual Action. The action taken depends upon the application. The concluding act is switching the FTRs in the Output Assemblies from Switch Pack Control to the CEOS control including power turn off via the system Mercury Contactor. The result for Traffic signal Control is Intersection is FLASH Mode and the Ramp Metering application is NO INDICATION or BLANK Mode.

7.1.5.2
SYSTEM MONITORING SYSTEM
The Cabinet Monitoring System is composed of Serial Bus #1, the Control/ Serial Bus Harnesses, the DC Power/COMM Assembly, the 212 Cabinet Monitor Unit with application DATAKEY resident in the DPA, Serial Bus #3 Harnesses interconnecting the output assemblies to the monitor (if required) and the 214 Auxiliary Monitor Unit(s) resident in all other output assemblies. The Communication criteria shall be 19,200 bps and asynchronous.

7.1.5.2.1
The AMU's role is to collect the output voltages of the 18/36 output switches and each switch pack current. It compares these readings to preset values and if exceeded, sets a associated bit with the switch and pack to "1" (otherwise set at "0"). Upon command from the CMU via Serial Bus #3 (using Standard Message SDLC Protocol) responds in a word/bit pattern. The CMU unit collects he associated bit states and does compare to values programmed in a Matrix Pattern located in the DATAKEY for conflict or other conditions. If the conditions match up, the unit shall activate the LFSA placing the cabinet in FLASH or BLANK operation or respond in a set program action. In addition to monitoring the AMU, the CMU shall monitor the Cabinet Power Supply Units directly and the ATC Unit via Serial Bus #1. Should the Power Supply Unit fail or there be an ATC/Serial Bus #1 COMM error, the unit shall place the cabinet in FLASH/BLANK operation.

7.1.5.3
Serial Bus #3 System – Serial Bus #3 is composed of the Model 212 Cabinet Monitor Unit (CMU) resident in the PDA, the Bus Harnesses daisy chained between the Output Assemblies and the PDA and the Model 214 Auxiliary Monitor Units (AMU) resident in the Assemblies. The Model 212 Monitor shall originate the Commands and the Auxiliary Monitor Unit(s) the Responses. The CMU/AMU addresses shall use the Output Assembly lsb and nlsb address lines. The addresses shall be as follows:

AMU/OA#1- 01, AMU/OA#2- 10, AMU/OA#3- 11 and AMU/OA#4- 00.

7.1.5.4
Serial Bus #3 Messages
Message 1 – SENSE COLLECTION COMMAND

BYTE	msb							lsb	FUNCTION
1	0	0	0	0	0	0	0	1	Message 1
2	R	C	x	x	x	x	x	x	control byte

R – RESET
C – Clear Values
Message 129 – SENSE COLLECTION RESPONSE

BYTE	msb							lsb	FUNCTION
1	1	0	0	0	0	0	0	1	Message 129
2	s1rv1	s1yv1	s1gv1	s2rv1	s2yv1	s2gv1	s1i1	s2i1	
3	s3rv1	s3yv1	s3gv1	s4rv1	s4yv1	s4gv1	s3i1	s4i1	
4	s5rv1	s5yv1	s5gv1	s6rv1	s6yv1	s6gv1	s5i1	s6i1	
5	s1rv2	s1yv2	s1gv2	s2rv2	s2yv2	s2gv2	s1i2	s2i2	
6	s3rv2	s3yv2	s3gv2	s4rv2	s4yv2	s4gv2	s3i2	s4i2.	
7	s5rv2	s5yv2	s5gv2	s6rv2	s6yv2	s6gv2	s5i2	s6i2	
8	FTRC1,FTRC2,FTRC, FTRC4,FU1,FU2,FU3,FU4								

s3rv1	**Switch Pack 3, Red, Voltage 1 (20 +/- 5 VAC RMS)**
s5yv2	**Switch Pack 5, Yellow, Voltage 2 (60 +/- 10 VAC RMS)**
s1i1	**Switch Pack 1, Current 1 (above 200 ma RMS)**
s2i2	**Switch Pack 2, Current 2 9above 100 ma RMS)**
fu1	**Flasher Unit 1**
FTRC1	**Flash Transfer Relay Coil**

7.1.4.5.2
Message 2 – REPORT / STATUS COMMAND

BYTE	msb							lsb	FUNCTION
1	0	0	0	0	0	0	1	0	Message Number
2	x	x	x	x	x	x	x	x	Status at present not assigned
3	x	x	x	x	x	x	x	x	Report Number

Message 130 – REPORT / STATUS RESPONSE

BYTE	nsb							lsb	FUNCTION
1	1	0	0	0	0	0	1	0	Message Number
2	x	x	x	x	x	x	x	x	at present not assigned
3-14									Report bytes

CHAPTER 7 - SECTION 2

HOUSINGS

7.2.1
HOUSING PACKAGE - The housings shall include, but not be limited to, the following:

Enclosure	**Gasketing**	**Police Panel**
Doors	**Ventilation**	**Cage Supports and Mounting**
Hinges and Door Catches	**Latches / Locks**	

7.2.2
HOUSING CONSTRUCTION - The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have front and rear doors, each equipped with a lock.

7.2.2.1
The enclosure and, doors, lifting eyes, gasket channels, police panel, and all supports welded to the enclosure and doors shall be fabricated of 3.175mm minimum thickness aluminum sheet. Bolted-on supports shall be of the same material and thickness as the enclosure or 2.667mm minimum steel. The side panels and filter shell shall be fabricated of 2.032mm minimum thickness aluminum sheet.

7.2.2.2
All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filled to a radius of .794mm minimum. Exterior cabinet welds shall be done by gas Tungsten arc TIG process only. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum. Internal cabinet welds shall be done by gas metal arc MIG or gas Tungsten arc TIG Process.

7.2.2.3
ALUMINUM SURFACES shall conform to the following:
An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning and etching procedure shall be to immerse in inhabited alkaline cleaner at 71°C for five minutes (Oakite 61A, Diversey 909 or equivalent in mix of the 6 to 8 ounces per gallon to distilled water). Rinse in cold water. Etch in a sodium solution at 66°C for 5 minutes 90.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mix per gallon to distilled water). Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 20°C for 2 minutes. Rinse in cold water. The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, class I Coating except the outer housing surface coating shall have a 0.01778mm minimum thickness and a 0.04186 milligrams per square mm minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution of nickel acetate 4 (pH 5.0 to 6.5) for 15 minutes at 99°C.

7.2.2.4
The enclosure doorframes shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 3.9624 (±2.032)mm.

7.2.3
GASKETING - Gasketing shall be provided on all door openings and shall be dust-tight. Gaskets shall be 6.35mm minimum thickness closed cell neoprene or silicone (BOYD R-108480 or equal) and shall be permanently bonded to the metal. If neoprene is used the mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A gasket top channel shall be provided to support the top gasket on the door to prevent gasket gravitational fatigue.

7.2.4
CAGE MOUNTING ANGLES - Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 4.775mm aluminum or 2.667mm steel.

7.2.5
LIFTING EYES - The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 19.05mm. Each eye shall be able to support the weight load of 909kg.

7.2.6
EXTERIOR BOLT HEADS - All heads shall be tamperproof type.

7.2.7
DOOR LATCHES AND LOCKS - The latching handles shall have provision for padlocking in the closed position. Each handle shall be 19.05mm minimum diameter stainless steel with a minimum of 12.7mm shank. The padlocking attachment shall be placed at 101.6mm from the handle shank center to clear the lock and key. An additional 101.6mm minimum gripping length shall be provided.

7.2.7.1
The latching mechanism shall be a three-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 6.35mm thick by 19.05mm wide minimum. Rollers shall have a minimum diameter of 22.225mm with nylon wheels and steel ball bearings. When the door is closed and latched, the door shall be locked. The locks and handles shall be on the left side of the front door and right side of the rear door. The locks on Housing #3 shall be centered in the middle of the cabinet. The lock and lock support shall be rigidly mounted on the door. In the locked position, the bolt

throw shall extend a minimum of 6.35 ± 7.9375mm into the latch Cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

7.2.7.2
The locks shall be Corbin 2 type or Best with dust cover. One key shall be supplied with each lock. The keys shall be removable in the locked position only. The locks shall have rectangular, spacing loaded bolts. The bolt shall have a 7.1374mm throw and shall be 19.05mm wide by 9.525mm thick (tolerance is +0.899mm).

7.2.7.3
The center latch cam shall be fabricated of a minimum thickness 4.7625mm aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.

7.2.8
HOUSING VENTILATION - Shall including intake, exhaust, filtration, fan assembly and environmental control as follows:

7.2.8.1
The louvered vent depth shall be a maximum of 6.35mm. A removable and reusable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 6.35mm to house the filter. The filter resident in its shell shall be held firmly in place with a bottom bracket and spring loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed into a waterproof sump with drain holes to the outside housing. The filter shall be 406.4mm wide by 304.8mm high by 22.225mm thick. The filter shall be an ECO-AIR Product E35S or equal. The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for Housing #1; 120 cubic feet of air per minute for Housing #3; and 26 cubic feet of air per minute for Housing #2

7.2.8.2
Each electric fan shall be equipped with ball or roller bearings and with a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the housing and vented.

7.2.8.3
The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 33°C and 65°C with a differential of not more than 6°C between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 10°C increment scale.

7.2.9
HINGES AND DOOR CATCHES - Two-bolt per leaf hinges shall be provided to bolt the enclosure to the door. Housing #1 and Housing #3 shall have four hinges and Housing #2

shall have three hinges. Housing #3 may use a continuous hinge in place of the leaf hinges when specified as single front and rear door option. Each shall be 88.9mm minimum length and have a fixed pin. The pin ends shall be welded to hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

7.2.9.1
Front and rear doors shall be provided with catches to hold the door open at both 90 and 165 ± 10 degrees. The catch minimum diameter shall be either 9.525mm for plated steel or aluminum rods or 6.35mm for Stainless Steel. The catches shall be capable of holding the door open at 90 degrees in a 60mph wind acting at an angle perpendicular to the plane of the door.

7.2.10
POLICE PANEL - A police panel assembly shall be provided to allow the police officers limited access to intersection control. The police panel assembly shall comprise of a cavity that is 13.5" wide 4.5" tall and 3" deep. Mounted on the front top center on Housing #3, see details for housings 1 and 2. The police panel shall have provision for four Toggle Power Switches. The panel door shall be equipped with a lock. The lock shall be keyed for a master police key. One key shall be furnished with each police lock. Each police key shall have a shaft at least 44.45mm in length.

Models 354 & 356 - One switch shall be labeled "ON - OFF LIGHTS" and the other "POLICE CONTROL ON-OFF". This assembly shall be capable of a manual plug and switch.

Models 340, 342, and 346 - One switch shall be labeled "ON - OFF" and the other "FLASH/AUTOMATIC".

Model 340 shall contain a manual plug and cord with a Manual Control Enable switch.

7.2.10.1
The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

7.2.10.2
The panel assembly shall have a drain to prevent water from collecting within the assembly. The drain shall be channeled to the outside.

CHAPTER 7 SECTION 3

CABINET CAGES

7.3.1
A standard EIA 19-inch (482.6mm) rack cage shall be installed inside the housing for mounting of the controller unit and cabinet assemblies. The EIA rack portion of the cage shall consist of 2 pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall be either 3.4163mm plated steel or 2.667mm stainless steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with standard EIA-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.

7.3.2
Clearance between rails for mounting assemblies shall be 450.85mm.

7.3.3
Two (2) steel supporting angles extending from the front to the back rails shall be supplied to support the controller unit. The angles shall be designed to support a minimum of 22.72kg each. The horizontal side of each angle shall be a minimum of 76.2mm. The angles shall be vertically adjustable. When a drawer is required these angles shall be part of the drawer assembly.

7.3.4
The cage shall be bolted to the cabinet at 4 points, via the housing cage supports and associated spacer brackets, 2 at the top and 2 at the bottom of the rails.

7.3.5
The cage(s) shall be centered within the cabinet.

CHAPTER 7 - SECTION 4

CABINET ASSEMBLIES

7.4.1 GENERAL

7.4.1.1
The cabinet assemblies shall be completely removable and installable from the cabinet without removing any other equipment and using only a Standard Slotted or Phillips screwdriver.

7.4.1.2
All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

7.4.1.3
LABELS and MARKER STRIPS - All equipment in the cabinet, when required shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.

7.4.1.4
Resistor-capacitor TRANSIENT SUPPRESSION shall be provided at all relay sockets (across relay coil) except for the Flash Transfer Relays (FTR) in the output assemblies where one suppression device may be common for all.

7.4.1.5
ASSEMBLY DEPTH DIMENSION shall include terminal sockets and strain relief bar.

7.4.1.6
All assemblies shall allow AIR CIRCULATION through its top and bottom unless specifically called out otherwise.

7.4.1.7
Connector types for assemblies shall be Manufacturer "or Equal" as follows:

MBP Signal AC Sockets	**BEAU S-5416-DB**
MBP Signal AC Plug	**BEAU P-5416-DB**
PDA Signal AC Power Socket	**BEAU S-5416-CCE**
Output Assembly AC Power Plugs	**BEAU P-5412-CCE**
Output Assembly AC Power Socket	**BEAU S-5412-DB**
Switch Pack Sockets	**BEAU S-5412-XX**
Line Filter Socket Polarizing pins 13 & 14	**BEAU S-5414-(SB-100-SA-1979)**
Heavy Duty Relay Sockets	**BEAU S-5408-XX**
Flasher Unit Socket	**BEAU S-5406-XX**

Serial Interface Unit (SIU)	**DIN 41612 standard C96 pin**
CMU and AMU Socket	**DIN 41612 standard C64 pin (a-b)**
Output Assembly Field Sockets	**Phoenix 7.62 mm (18-61-19-6) 6 pin**
Output Assembly Mating Field Plugs	**Phoenix 7.62 mm (18-04-91-7) 3 pin**
Output Assembly Mating Field Plugs	**Phoenix 7.62 mm (18-04-94-6) 6 pin**
Output Assembly Mating Field Plugs	**Phoenix 7.62 mm (18-40-15-9) 6 pin**
Output Assembly Transient socket	**Phoenix 5.08 mm (07-10-24-8) 9 pin**
Output Assembly Transient plug	**Phoenix 5.08 mm (17-57-08-0) 9 pin**
Input/Output Assembly Address Sockets	**Phoenix 3.81 mm (18-27-59-6) 8 pin**
Input/Output Assembly Address Plug	**Phoenix 3.81 mm (18-27-76-1) 8 pin**
Input Assembly Field Sockets	**Phoenix 5.08 mm (17-55-81-7) 10 pin**
Input Assembly Field Plugs (screw lug)	**Phoenix 5.08 mm (17-57-09-3) 10 pin**
Input Assembly Field Plugs (screw lug)	**Phoenix 5.08 mm (17-57-04-8) 5 pin**
Input Assembly Field Plugs (screw lug)	**Phoenix 5.08 mm (18-53-04-9) 5 pin**
Input Assembly Field Plugs (crimp pin)	**Phoenix 5.08 mm (18-08-89-0) 10 pin**
MBP DC bus socket	**BEAU S –3304 -DB**
MBP DC bus plug	**BEAU P –3304 –DB**
PDA DC bus Socket	**BEAU S-3304-CCT**
All Assemblies DC bus Plug	**BEAU P-3304-CCT**
All Assemblies Comm Bus socket	**SB1 and SB2 DB 25 Female with AMP latching block**
All Assemblies Comm Bus SB1 and SB2 Plug	**DB 25 with AMP spring latch**
All Assemblies Monitor Comm Bus socket	**SB3 Dual RJ45 Cat 5 pin out.**
All Assemblies Power Plug	**NEMA 5-15-P**
MBP AC Filtered Bus socket	**NEMA 5-15-R**
MBP Filtered Bus receptacle	**IEC - 320 Male recessed Receptacle**
Filtered Bus Interface Cord	**IEC -320 Male to Female Cord.**
Filtered Bus interface PDA	**Dual IEC - 320 Female Receptacle CP1**
Input Assembly Test Port	**37 Pin "D" Female Receptacle TP1**
Output Assembly Test Port	**25 Pin "D" Male Plug. TP2**
PDA, Input and Output Assembly ISO port.	**9 Pin "D" Male Plug ISO1**

7.4.1.8

Connector SOCKETS for Flasher and Switchpack Units shall be mounted with their front face 190.5mm from the assembly front panel.

7.4.1.9

NYLON GUIDES (top and bottom) shall be provided for Switchpack and Flasher Units, Monitor Units, Serial Interface Units, Detector Sensor and Isolator Units and Power Supply Units (bottom only). The guides shall begin 25.4 12.7mm from the connector socket face.

7.4.1.10

Assemblies shall be FABRICATED of 15.24mm minimum thickness aluminum or stainless steel sheet. The aluminum metal surface shall be treated with clear chromate.

7.4.2 CABINET DRAWER ASSEMBLY

A rail mounted shelf unit shall be supplied to support the Controller Unit. The shelf unit shall be designed to support the drawer assembly and be vertically adjustable as a unit.

7.4.3 POWER DISTRIBUTION ASSEMBLY

There are two Power distribution Assemblies, PDA #5 and PDA#6. PDA use and mounting depends upon required application. See Chapter 7, Section 1.

7.4.3.1

PDA – The following equipment shall be provided

Duplex NEMA 5-15R Equipment Receptacle with GFI (on rear panel)
Single NEMA 5-15R Auxiliary Receptacle (on the front panel)
1 Pole 60 Amperes minimum (Airpax IEL Magnetic medium trip) 120V AC Main Circuit Breaker
1 Pole 15 Amperes minimum Magnetic 120V AC Service Breaker
2 Pole 20 Amperes minimum Magnetic 120V AC Flash Bus Breaker
1 Pole 15 Amperes minimum Magnetic 120V AC with Auxiliary Switch feature, Signal Bus Breakers.
AUTO/FLASH switch
SIGNAL ON/OFF switch
FLASH indicator light
Filtered power 10 Ampere Fuse and holder
(1) Filtered power Indicator
(1) 115VAC 1 form C SPDT relay (eq. Midtex Type 158) and socket for flash sense indicator.
Mercury Contactor (NO) normally open, rated at 60 Amperes, 120V AC
Type 204 Flasher sockets
Total, 1Type 216A +24V DC and 1 Type 216B +12V DC Power Supplies and sockets
IEC - 320 Dual Female Receptacle (CP1) Filtered Power source
Surrestor for TBS
(1) 10 Amp Filter CORCOM 10VS1 or Optional EDCO SHA – 1250 (Pluggable Assembly) and socket.
(3) HDFK 25 Phoenix Contact through panel terminals for TBS1 (07-07-743)
(3) VDFK 6 Phoenix Contact through panel terminals for TBS2 (07-11-027)
Molex type 3191-15 panel mount connector (CI-1) cabinet interface
18 inch DC power Cord with BEAU S –3304 -CCT socket.
18 inch AC Signal power Cord with BEAU S-5416-CCE socket.
(1) 24VDC 1 form C SPDT relay (eq. Midtex Type 258) and socket for Monitor Interconnect.
25 position "minimum copper bus terminal for AC - termination for the signal bus. This bus shall be isolated from the assembly.
9 Pin “D” Connector Male Plug ISO1 for Cabinet Control signal interface.
(1) Phone Jack for Monitor Testing.
25 Pin “D” Connector Female for SB1/SB2 Serial Interface.
Dual RJ45 Sockets for Serial Bus 3 Interconnect.

7.4.3.2
Fixed 10 Amp filter shall be a Corcom 10VS1 or equal.
The SHA-1250 filter connector shall be installed within the PDA such that minimal wire length is needed between cabinet input power (TBS1) and filter/conditioning unit. TBS1, and TBS2, shall be wired and provided as shown on drawings.

7.4.3.3
The Circuit Breaker fault condition for the eight field breakers shall be accomplished by eight independent breakers equipped with a switch, attached to the rear of each breaker, that will respond to the breaker "Trip" condition. When the breaker is tripped the switch will open the path between the Monitor LFSA contacts the Mercury Contactor Coil and the Flash Transfer Relays. In a "Trip" condition the result will be flashing indication in the field. The CMU will sense this condition at pin A23 "CB Trip Status".

7.4.3.4
Rating of breakers shall be shown on the face of the breaker or handle. Breaker function shall be labeled below the breakers on the front panel.

7.4.3.5
The rear ground fault receptacle shall have ground-fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur on 6ma of ground fault-current and shall not occur less than 4ma of ground-fault current. The ground-fault receptacle shall provide the single plug on the front panel power via the expansion terminal.

7.4.3.6
The AUTO/FLASH Switch when placed in FLASH position (down) shall de-energize the Mercury Contactor (MC) coil and Flash Transfer Relay coils. When the switch is placed in the AUTO position (up) the coils will be energized and the Switchpacks shall control the signal indications. The switch shall be a SPST Toggle Control Switch.

7.4.3.7
The FLASH Indicator light labeled "Flash On" shall be mounted on the PDA front panel. The Flash Relay Circuit No.1 shall drive the lamp through the Flash Sense Relay. This relay coil shall be attached to the FTR coil line of the PDA #5. When the system is switched to FLASH the relay will de-energize and operate the "Flash On" lamp.

7.4.3.8
The Cabinet Power Supplies shall be attached to the MBAP through an 18 inch cord and plug socket. The Plug socket shall be a BEAU S –3304 CCT. The cord shall be held by a strain relief upon exiting the assembly and wired to the Power Supply Sockets within the PDA#5

7.4.3.9
Ganged Circuit Breakers shall be assembled by the circuit breaker manufacturer and certified that their circuit breakers shall gang trip.

MODULAR BUS ASSEMBLY PACKAGE

7.4.4.1
The Modular Bus Assemblies shall be removable for maintenance and testing by the use of tab locks and supported by the side rail.

7.4.4.1
The AC+ Modular Dual Bus Assembly shall provide AC power to the switch packs and flasher power to the FTR's in the Output Assembly. The Signal Bus shall contain a minimum of four BEAU S-5412-DB outlets and one BEAU P-5416-DB socket. Outlet spacing shall be 5.25-inch minimum.

7.4.4.2
Wire rating within the bus shall be a minimum of #14 AWG (1.63 mm) wire, for all Switchpack and flasher and signal pins. Signal pins shall be a minimum 18 AWG (1.02 mm).

7.4.4.3
Each 12 pin Output Assembly outlet shall provide two 15-ampere Switchpack lines. Each of the Switchpack lines shall be attached to an individual 15-ampere circuit breaker located in the PDA via the PDA socket. Line distribution shall be successive, outlet 1, breaker 1 and 2, outlet 2, breaker 3 and 4, outlet 3, breaker 5 and 6, outlet 4, breaker 7 and 8.

7.4.4.4
Each 12 pin outlet shall provide four flasher lines, FL1+, FL 1-, FL2+ and FL2-. Each of the outlets shall have specific flasher assignments. Outlets 1 and 3, pin 3 (FL1+) pin 4 (FL1-) pin 5 (FL2+) pin 6 (FL2-). Outlets 2 and 4, pin 3 (FL1-) pin 4 (FL1+) pin 5 (FL2-) pin 6 (FL2+).

7.4.4.5
Outlet pins 7-12 shall be wired as follows:
Flash Transfer Relay Coil Drive
AC+ MAIN
AC- MAIN
AC- MAIN
EQ. GND
EQ. GND

7.4.4.6
The PDA plug shall be a BEAU P-5416-DB or equivalent. Plug spacing shall be 5.25 inches (133.35mm) below the last Output Assembly outlet.

7.4.4.7
Pin Assignment for the PDA plug shall be:
CB1 AC+
CB2 AC+
CB3 AC+
CB4 AC+
CB5 AC+
CB6 AC+
CB7 AC+
CB8 AC+
Flasher 1 +
Flasher 1 –
Flasher 2 +
Flasher 2 –
EQ. GND
Flash Transfer Relay Coil Drive
AC+ MAIN
AC- MAIN

7.4.4.8
The (filtered) assembly shall provide clean AC power the rack assemblies. Each bus shall contain a minimum of seven NEMA 5-15R outlets with isolated ground pin construction. This bus shall connected to the CP1 outlet on the PDA by means of a harness.

7.4.4.9
Outlet Spacing shall be 5.25 (133.35mm) inches minimum.

7.4.4.10
Signal wire size shall be a minimum of 18AWG (1.02 mm0)

7.4.4.11
The DC Power and Communications Bus shall contain the +24VDC and +12VDC cabinet DC power source. The bus shall contain eight +12/+24VDC outlets. The DC outlets shall be BEAU S –3304 -DB

7.4.4.12
Outlet Spacing shall be 5.25 inches (133.35mm) minimum.

7.4.4.13
Signal wire size shall be a minimum of #18AWG(1.16mm) wire for DC signals. DC power and ground wires shall be a minimum of #14 AWG (1.85mm)

7.4.4.14
Signal Description shall be as follows:
+24VDC
DC Ground

+12VDC
DC Ground

7.4.4.15
Communications Bus: The bus shall contain a minimum of nine DB 25 outlets using 12 pairs of UTP CAT 5 wire interconnect. This bus shall connected to the ATC and other devices by means of a Harness. Harness wires shall be provided for each of the Rack Assemblies.

7.4.4.16
Outlet spacing shall be a minimum of 5.25 inches.

7.4.4.17
Signal wire shall be #24AWG (0.97mm) UTP CAT 5 wire minimum.

7.4.4.18
Signal assignment for the shall be:

(1) SP1 TX+	**(14) SP1 TX-**
(2) SP1 RX+	**(15) SP1 RX-**
(3) SP1 TXC+	**(16) SP1 TXC-**
(4) SP1 RXC+	**(17) SP1 RSC-**
(5) SP2 TX+	**(18) SP2 TX-**
(6) SP2 RX+	**(19) SP2 RX-**
(7) SP2 TXC+	**(20) SP2 TXC-**
(8) SP2 RXC+	**(21) SP2 RXC-**
(9) LINESYNC+	**(22) LINESYNC-**
(10) NRESET+	**(23) NRESET-**
(11) PWRDWN+	**(24) PWRDWN-**
(12) +5VDC*	**(25) +5VDC Max current 100 ma**
(13) DC GND #2	

7.4.4.19
The Modular Bus Assemblies shall be the plug/outlet facilities within the cabinet racks to provide communications, DC power, AC power and Clean AC power to the Distribution, Input and Output assemblies and other devices that will be introduced to the ITS cabinet facility. These assemblies are fastened by way of hooks and screws to the rack rails. Side panels shall be designed to accommodate the hooks. The details contain the construction of the panels.

7.4.4.20
Modular Bus Assembly side panels that support the Signal and Filtered AC shall contain a 12 position copper bus for attaching the Equipment Ground cables to the Input and Output Assemblies.

7.4.5 INPUT ASSEMBLY

7.4.5.1
The Input Assembly shall be a rack-mountable module, which will provide an interface between input devices such as transportation sensor units and the advanced controller unit. This shall be accomplished by a combination of back-plane wiring and parallel interface wiring to the advanced controller unit. In addition, provision shall be made to readily accommodate a Serial Interface Unit (SIU). Field inputs will be directly terminated on the back of the Input Assembly.

7.4.5.2
The Input Assembly shall consist of an input section, which can support up to twelve input devices, parallel wiring to the advanced controller unit through the SIU (Serial Interface Unit) which shall be provided. An additional test interface to a parallel wiring harness attached to an AMP 37 pin type "D" male bulkhead connector.

7.4.5.3
The SIU will be the device that converts all input to a serial message for routing to the advanced controller unit. The SIU shall also be able to reset any of the input devices. Multi-drop communications between the SIU and the input devices shall be provided. Individual reset lines to each input device shall also be a function requirement. Serial Communication shall be provided through a 25-Pin female "D" connector located on the rear panel. Serial Port 1 and Serial Port 2 shall be attached to the Input Assembly SIU. Interconnect between the 25 Pin "D" connector shall be with CAT 5 UTP wire.

7.4.5.4
The Input Assembly shall utilize 133.35mm of rack height.

7.4.5.5
The assembly will be 444.5mm wide and mountable in a 19 inch (482.6mm) rack.

7.4.5.6
The assembly shall allow air circulation through the top and bottom.

7.4.5.7
The assembly shall provide nylon card guides (top and bottom) and a 22 pin dual readout, edge connector centered vertically for each of the 12 input devices.

7.4.5.8
The SIU slot width shall be a maximum 57.15mm. Each input device slot width shall be a maximum 28.575mm.

7.4.5.9
All power and communication connections shall be on the back of the Input Assembly.

7.4.5.10
One NEMA 5-15 plug and cord shall be provided for input of 115V AC filtered power for use with input devices. The NEMA 5-15 plug and cord shall be wired to the back plane as

follows: Chassis ground (pin L), AC- (pin M) and AC+ (pin N) common on all twelve input devices.

7.4.5.11
One BEAU S –3304 -CCT socket attached to a 18-inch cable shall be supplied for interconnect of the +24 VDC and +12 VDC power.

7.4.5.12
Interconnect of the four optically isolated inputs on the SIU, shall be provided on the rear panel. By means of a DB9 Male Connector. Pin assignment shall be as follows:

OI-1
OI-2
OI-3
OI-4
OI-COMMON
Reserved
Reserved
Reserved
Reserved

AC Reference and AC Reference Common are pins reserved for applications using BIU type of devices.

7.4.5.13
The Input Assembly shall inter-mate with and support 12 dual-channel loop detector units. Support shall be provided for up to 24 inputs. The Input Assembly shall support two-channel and four-channel input devices. Two-wire field input plus an earth ground termination will be provided for each channel of the Input Assembly. Rack and slot addressing shall be provided.

7.4.5.14
The Input Assembly will support existing NEMA and TYPE 170 Input devices such as Model 222 and 224 Loop Detectors, Model 242 DC Isolators, Model 252 AC Isolators, Model 255 Railroad Isolators, Emergency Vehicle Preemption Isolators, and other rack mountable input devices compatible with NEMA and TYPE 170 specifications.

7.4.5.15
The +12 VDC at 100ma (minimum) and 120V AC at 100ma (minimum) power will be made available to all input devices on the back plane. All input devices shall have individual rest lines. Reset line assignment from the SIU to the 12 input device slots shall be: (Slot / SIU pin)

1. **Slot #1 A2 OUTPUT 1**
2. **Slot #2 B2 OUTPUT 2**
3. **Slot #3 A3 OUTPUT 3**

4. Slot #4 B3 OUTPUT 4
5. Slot #5 A4 OUTPUT 5
6. Slot #6 B4 OUTPUT 6
7. Slot #7 A5 OUTPUT 7
8. Slot #8 B5 OUTPUT 8
9. Slot #9 A6 OUTPUT 9
10. Slot #10 B6 OUTPUT 10
11. Slot #11 A7 OUTPUT 11
12. Slot #12 B7 OUTPUT 12

7.4.5.16
Pins D, E, J, K, and L on each edge connector slot shall be terminated on their associated field terminal by connection to the 10 position Field Sockets.

7.4.5.17
Transient Protectors shall provide AC protection and DC protection. These devices shall be provided on the side panel of the Rack Assembly.

7.4.5.18
Earth-ground shall be provided to each of the twelve (12) ten position sockets via a screw lug terminal mounted on the rear panel. The screw lug terminals shall face to the right when viewed from the rear of the assembly.

7.4.6.19
Each Input Assembly field termination shall be equipped with two five position screw lug plugs for direct connection of the field wires or two five position crimp pin connectors with a cable attached to the Rack Side Panel.

7.4.5.20
Each Input Assembly shall contain a 4 bit address code plug and socket. The Input Assembly address shall be provided by a plug with jumpers installed to produce a binary code 1, 2, 4, and 8. Pins 1 (1), 3 (2), 5 (4) and 7 (8) shall represent the code. Pins 2, 4, 6 and 8 shall be common to the SIU common pin for the address inputs. The address receptacle shall be installed on the back panel of the Input Assembly, see connector list. A plug shall be provided, that may be factory or technician programmed and shall mate with the address receptacle, see connector list.

7.4.5.21
A DIN 41612 standard C96 pin socket shall be provided in the center location of the Input Assembly for the SIU.

7.4.5.22
The edge connectors for the 12 input devices shall be double-sided connectors with the number side of each pin as shown on the drawings provided in this specification.

7.4.5.23
The pin termination of the 37-pin (*25pin) male* connector attached to the rear panel shall be as follows:

B13	**IN1**
A14	**IN2**
B14	**IN3**
A15	**IN4**
B15	**IN5**
A16	**IN6**
B16	**IN7**
A17	**IN8**
B17	**IN9**
A18	**IN10**
B18	**IN11**
A19	**IN12**
B19	**IN13**
A20	**IN14**
B20	**IN15**
A21	**IN16**
B21	**IN17**
A22	**IN18**
B22	**IN19**
A23	**IN20**
B23	**IN21**
A24	**IN22**
B24	**IN23**
A25	**IN24**
A32	**DCGND**

This connector shall be used to link parallel inputs tied to the SIU from each of the twelve input devices for use as a test cable or detector switch panel.

7.4.5.24
The nylon card guides shall begin within one inch of the front face of the file.

7.4.5.25
The input file shall be provided with marker strips to identify the isolators and detectors in the file.

7.4.5.26
An earth-grounding stud shall be provided on the lower right side of the field termination panel. The stud shall be #10 with a 10-32 wingnut.

7.4.5.27
INBUS System Requirements

7.4.5.27.1

The assembly SIU shall function as control master for the INBUS System via its Serial Port #3. The Bus shall interface using EIA 465 driver/ receiver full duplex multi drop. The command pair shall carry SIU Transmit messages to the 12 slot connectors/ detector sensor units. The response pair shall carry the addressed detector sensor unit response transmitted message back ro the SIU. The system baud rate shall be 19.2 KHZ.

The message format , number and command/ response shall be as follows:

Message Byte	Command	Response	Comment
1	ADDR Bits 1-4	ADDR Bits 1-4	HEADER 1
	MSS Bits 5-8	MSS Bits 5-8	
2	Same as Byte 1	Same as Byte 1	HEADER 2
3	Message Command Byte	Message response	First Byte
4-16		Message Response	Ensuing Bytes

MESSAGE 0 Detector Reset and/ or Status

MESSAGE 1

MESSAGE "0" ADDRESS "F" — **No response** — **All Detectors Reset**

MESSAGE "0" ADDRESS "x"

"00" — **individual detector Reset**

Detector Status individual Det response

Bit 1 "1"-doing reset, "0"- Cant

Bit 2 "1"- Open Loop Channel 1

Bit 3 "1"- Open Loop Cjannel 2

Bit 4 "1' Shorted LoopChannel1

Bit 5 "1" shorted Loop Channel 2

Bit 5 "1' - Low Q

Bit 6 "1"- Traking problems

Bit 7 "1"- Event Occurred

Bit 8 "1'-

3 — **"FF"** — **NoReset Only Status**

MESSAGE "1" ADDRESS "x"

7.4.6 OUTPUT ASSEMBLY

7.4.6.1

The Output Assembly shall be an EIA nineteen inch rack mounted assembly that will provide interface between the Advanced transportation controller unit and the proposed SIU (Serial Interface Unit) assembly, or parallel link to individually switch on and off the outputs of six switch pack devices. In addition to the SIU and switch pack devices, this module will provide a means for flash transfer of the switch pack outputs, monitor voltage

at the Output Assembly's field terminals, and threshold measure the switch pack current. The field outputs will be directly terminated on the back of the output assembly.

7.4.6.2
Three flash transfer relays shall be provided with six Flash Program Blocks to control red / yellow flash output. The flash programming connectors shall be Molex Type 1375 or approved equal. The receptacle shall be mounted on the Output Assembly with a jumper wire programmable plug connected to the corresponding red and yellow circuitry. Plug connectors, with respective jumper wires, shall be provided for each circuit to allow red or yellow flash programming. Plug Pins shall be crimped and soldered.

7.4.6.3
The three flash transfer relays shall be heavy-duty type. The coil of each flash transfer relay shall be de-energized when signals are in flashing operation and the police panel ON / OFF switch is ON. The relays shall transfer the field outputs from Switchpack output to flash control. The transfer shall not interrupt controller operation.

7.4.6.4
A SIU (Serial Inter face Unit) for control of outputs, and resident communications interface between the controller unit and the monitor shall be provided.

7.4.6.5
Serial Communications shall be provided through a female 25 Pin "D" connector located on the field termination panel. Serial Port 1 shall be attached to the Output Assembly SIU and Monitor connector. Serial Port 3 (Monitor Port) shall be connected to the Monitor connector. The female 25 Pin "D" connector shall be equipped with AMP latch blocks 0.090mm panel 7470802 or 0.60mm panel 7453453 or equal. Interconnect between the 25 Pin "D" connector shall be with CAT 5 UTP wire.

7.4.6.6
The Output Assembly field termination shall have three nine-pin sockets for Input Protection devices mounted on the panel. Wiring for these devices shall be listed in the connector drawings.

(1) Switchpack red	**(4) Switchpack green**	**(7) Switchpack yellow**
(2) Common AC -	**(5) Common AC -**	**(8) Common AC -**
(3) Switchpack yellow	**(6) Switchpack red**	**(9) Switchpack green**

7.4.6.7
The Output Assembly field termination shall be made up of six through-panel 20 ampere 7.62mm pitch, six pin sockets, see connector list. Additionally, three nine-pin 0.508mm pitch sockets for Input Protection devices shall be mounted on the panel. Wiring for these devices shall be listed in the connector drawings.

7.4.6.8
Each Output Assembly shall contain a 4 bit address code plug and socket. The Assembly address shall be provided by a plug with jumpers installed to produce a binary code 1, 2, 4 and 8. Pins 1 (1), 3 (2), 5 (4), and 7 (8) shall represent the code. Pins 2, 4, 6 and 8 shall be common to the SIU common pin for the address inputs. The address receptacle shall be installed on the field termination panel, see connector list. A plug shall be provided, that may be factory or technician programmed and shall mate with the address receptacle, see connector list.

7.4.6.9
The field termination panel shall include a strain relief support for field wires. Strain relief for field wiring shall be provided by stamped / pressed metal work on the rear panel. Tie-wraps shall then be used to provide strain relief. The switch pack number and circuit (G, Y, R) shall be silk-screened on the rear of the swing down panel, next to the field terminal blocks.

7.4.6.10
The field termination support panel shall include a DC power cable for cabinet +24V DC and +12V DC shall be a

+24 VDC
DC Ground
+12 VDC
DC Ground

7.4.6.11
The field termination support panel shall provide egress for a cable that will provide AC signal power and flasher control and power to the Output Assembly. This cable shall terminate with a BEAU P-5412-CCE connector, or approved equal, to be attached to the AC Power Bus.

The receptacle shall be wired to the Monitor Outlets 1 and 3: pin 3 (FL1+), pin 4 (FL1-), pin 5 (FL2+), pin 6 (FL2-).

Outlets 2 and 4: pin 3 (FL1-), pin 4 (FL1+), pin 5 (FL2-), pin 6 (FL 2+).

Outlet pins 7-12 shall be wired as follows:

Flash Transfer Relay Coil Drive
AC+ MAIN
AC- MAIN
AC- MAIN
EQ. GND
EQ. GND

7.4.6.12
A twenty-five pin male connector, DB25 male connector shall be provided to connect the Output Assembly to a cabinet test panel. The pin out shall be:

1. A2 OUTPUT 1
2. B2 OUTPUT 2
3. A3 OUTPUT 3
4. B3 OUTPUT 4
5. A4 OUTPUT 5
6. B4 OUTPUT 6
7. A5 OUTPUT 7
8. B5 OUTPUT 8
9. A6 OUTPUT 9
10. B6 OUTPUT 10
11. A7 OUTPUT 11
12. B7 OUTPUT 12
13. A8 OUTPUT 13
14. B8 OUTPUT 14
15. A9 OUTPUT 15
16. B9 OUTPUT 16
17. A10 OUTPUT 17
18. B10 OUTPUT 18
25. A32 DC GROUND

7.4.6.13
The Output Assembly shall be provided with marker strips on the front to identify load switch assignment when mounted in the file.

7.4.6.14
All of the switch pack sockets shall have pin 11 bussed together and connected to AC-.

7.4.6.15
Pin 4 on all switch pack sockets shall be bussed together and connected to logic ground. This will allow switch packs equipped with led indicators on the inputs and outputs.

7.4.6.16
Guides (top and bottom) shall be provided to support the switch packs.

7.4.6.17
Flash transfer relays shall be accessible on the Output Assembly without the use of tools or removal of any other equipment.

7.4.6.18
Six (6) Current Monitor coils shall be provided for current monitoring. Each coil measures individual switchpack current. The six AC input wires shall be routed through the coils, then

attached to the switchpack connectors. The two-wire outputs or the coils shall be routed to the AMU connector via a wire-to-wire cable connection.

7.4.6.19
Each current sensing coil shall be connected to the monitor connector via a two position 0.100 pitch wire-to-wire crimp housing Molex part number (50-57-9202) or equivalent. The connector shall be two position wire-to-wire 0.100 pitch Molex connectors, part number (70107-0001) or equivalent. The connector shall be wired to the AMU connector of the Output Assembly.

7.4.6.20.1 Physical Requirements: See details.

7.4.7 HARDWARE REQUIREMENTS

7.4.7.1
The Output Assembly shall contain the necessary plugs, mounting and termination facility necessary to operate the following devices.

1. Up to six NEMA Load Switch or 170 Switch Pack devices.
2. One SIU (Serial Interface Unit)
3. One SMU (Signal Monitor Unit) or one AMU (Auxiliary Monitor Unit)
4. Up to three FTR High Power Flash Transfer Relays
5. Six flash program block receptacles, two for each of the FTR relays
6. Six red flash program plugs
7. Four yellow flash program plugs
8. Three white or "non-flash" program plugs.

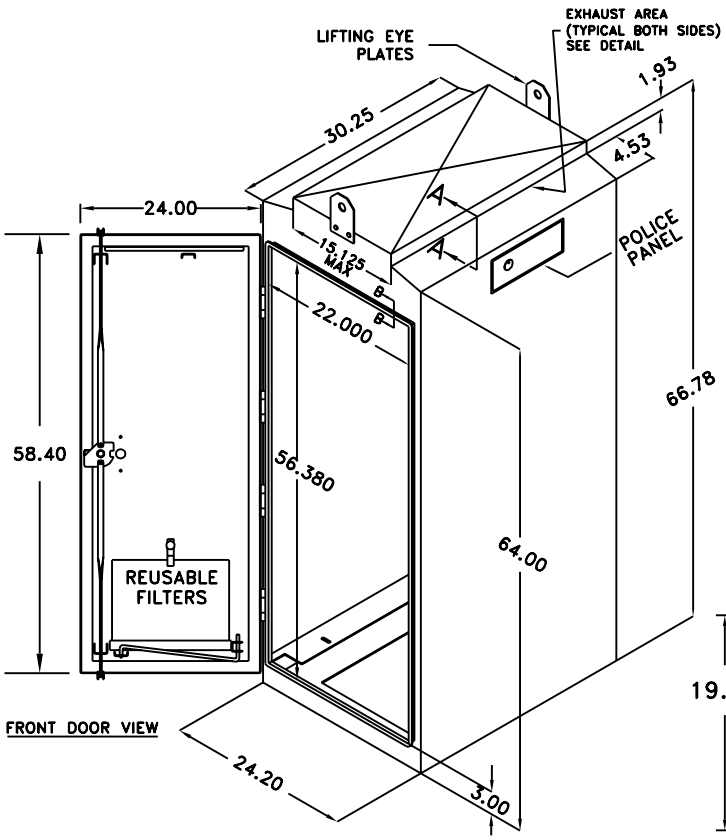
Note: The four-bit address code plug requirement shall be determined by the type and position of the individual assemblies.

CHAPTER 7 SECTION 5

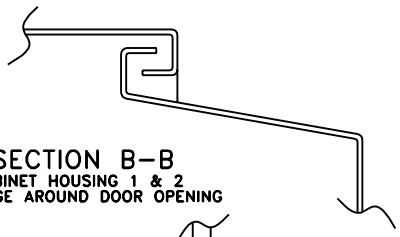
CABINET DETAILS

TABLE OF CONTENTS

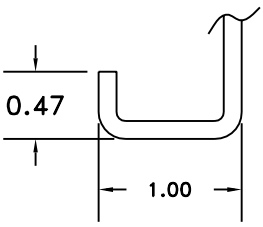
CABINET HOUSING 1 DETAIL



SECTION A–A
CABINET HOUSING 1 & 2
VENTILATION EXHAUST DETAIL

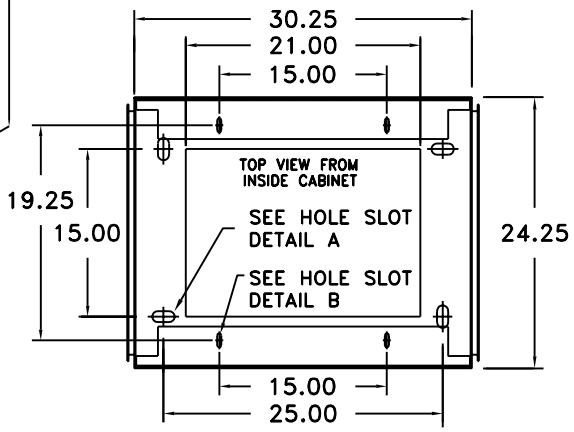


SECTION B–B
CABINET HOUSING 1 & 2
FLANGE AROUND DOOR OPENING

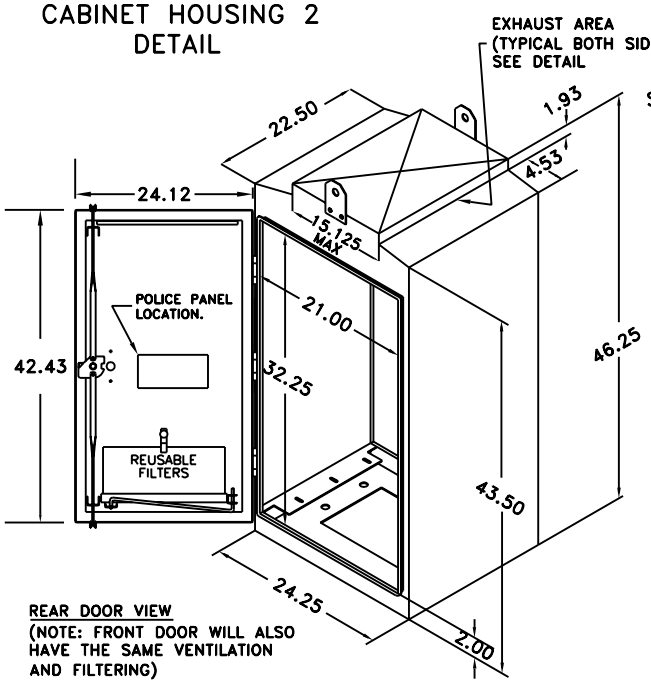


NOTE: ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.

CABINET HOUSING 1 BOTTOM DETAIL

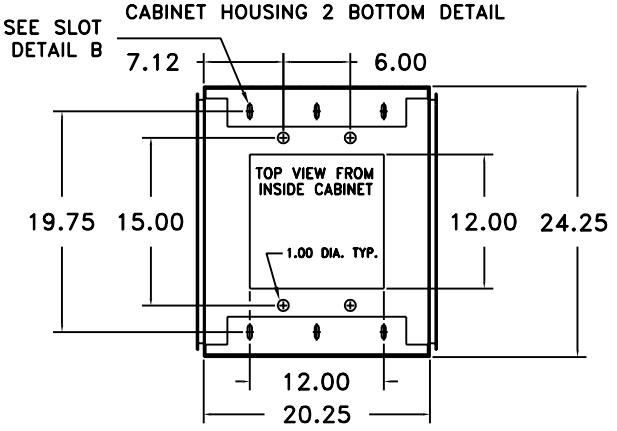


CABINET HOUSING 2 DETAIL



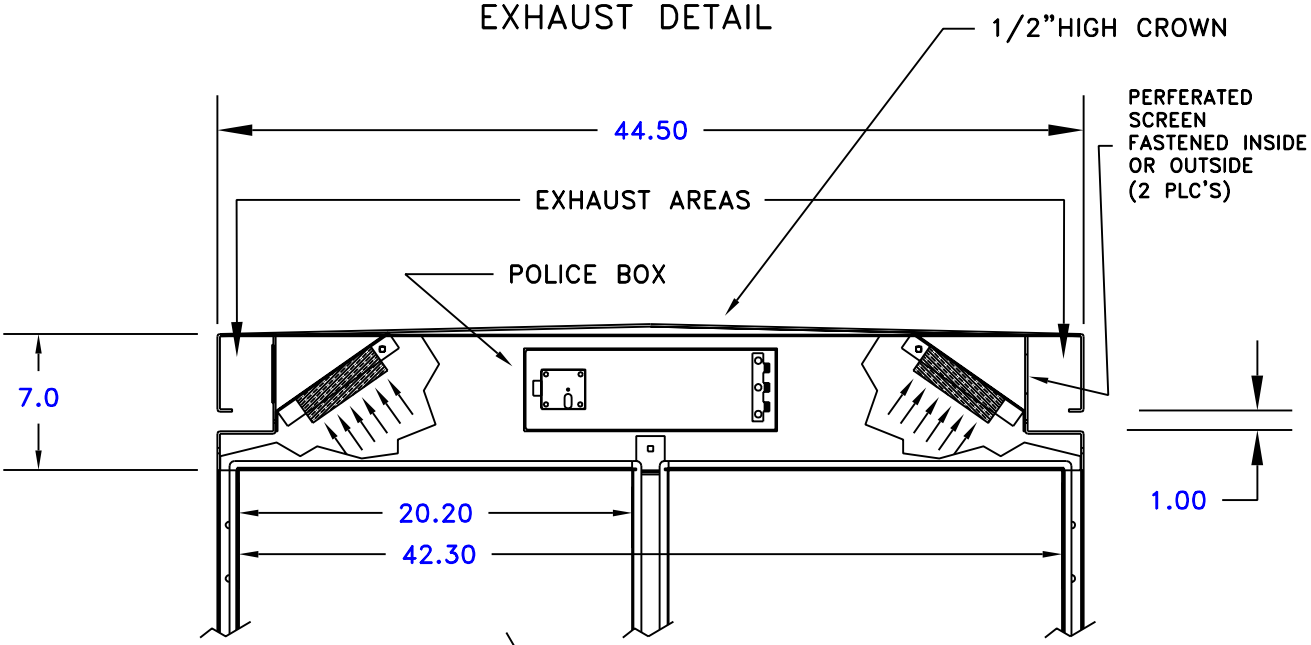
REAR DOOR VIEW
(NOTE: FRONT DOOR WILL ALSO HAVE THE SAME VENTILATION AND FILTERING)

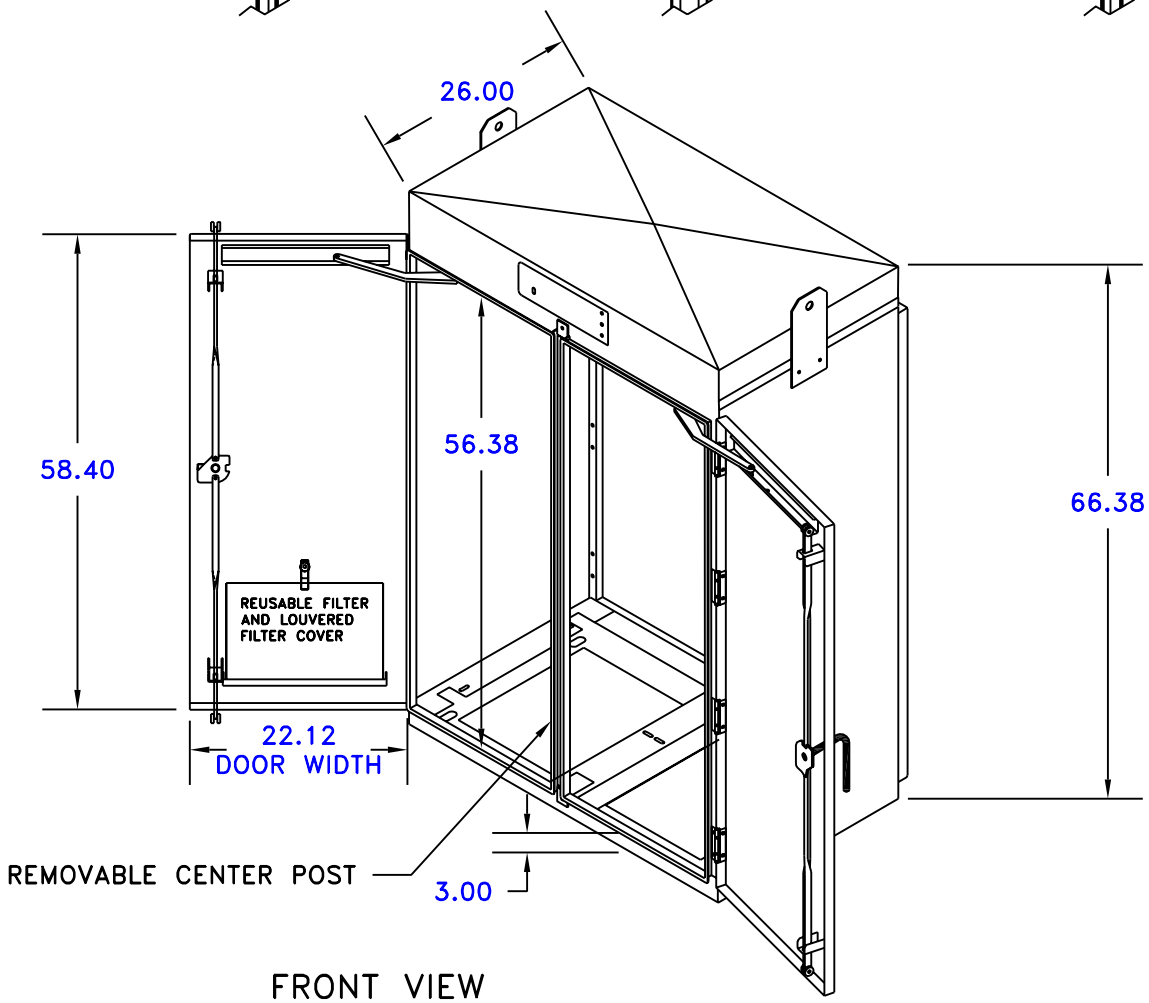
CABINET HOUSING 2 BOTTOM DETAIL



TITLE: CABINET HOUSING #1 & #2	
NO SCALE	
TEES, NOV 19, 1999	7-5-1

EXHAUST DETAIL

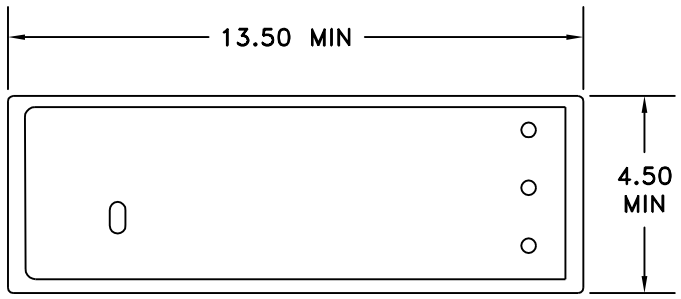




FRONT VIEW

TITLE: ITS/ATC CABINET ASSEMBLY HOUSING #3 DETAIL 1		
	NO SCALE	
	TEES, NOV 19, 1999	7-5-2

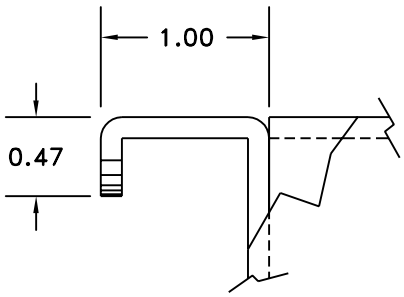
POLICE BOX DETAIL



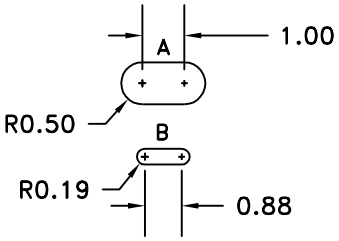
POLICE BOX TO BE A MINIMUM OF 3.00" DEEP

SECTION B–B

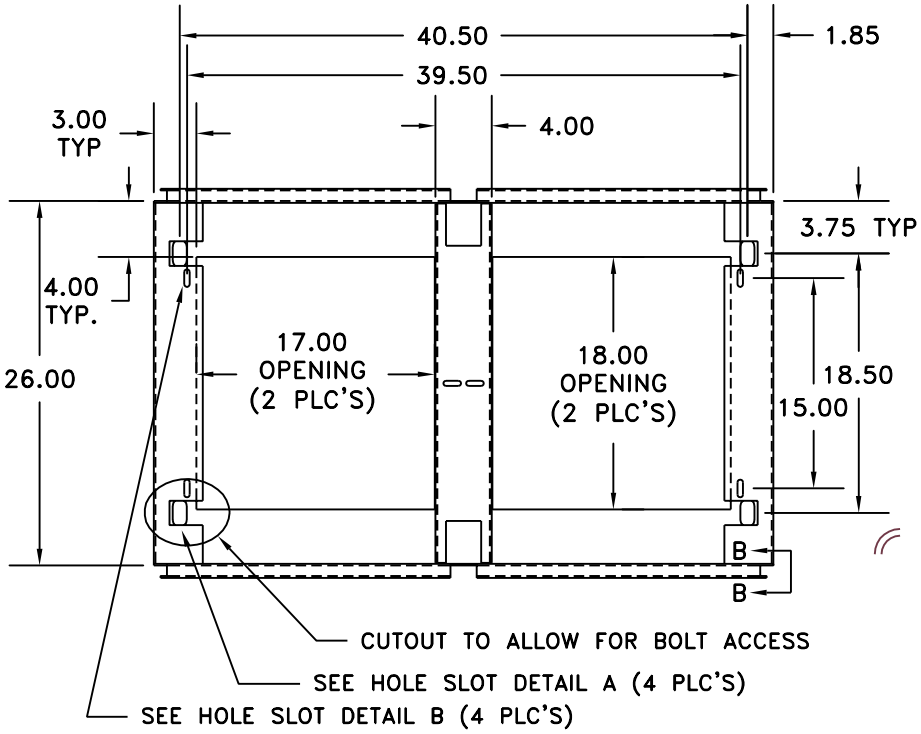
HOUSING 3 FLANGE
AROUND DOOR OPENING



HOLE SLOT DETAIL



BOTTOM DETAIL



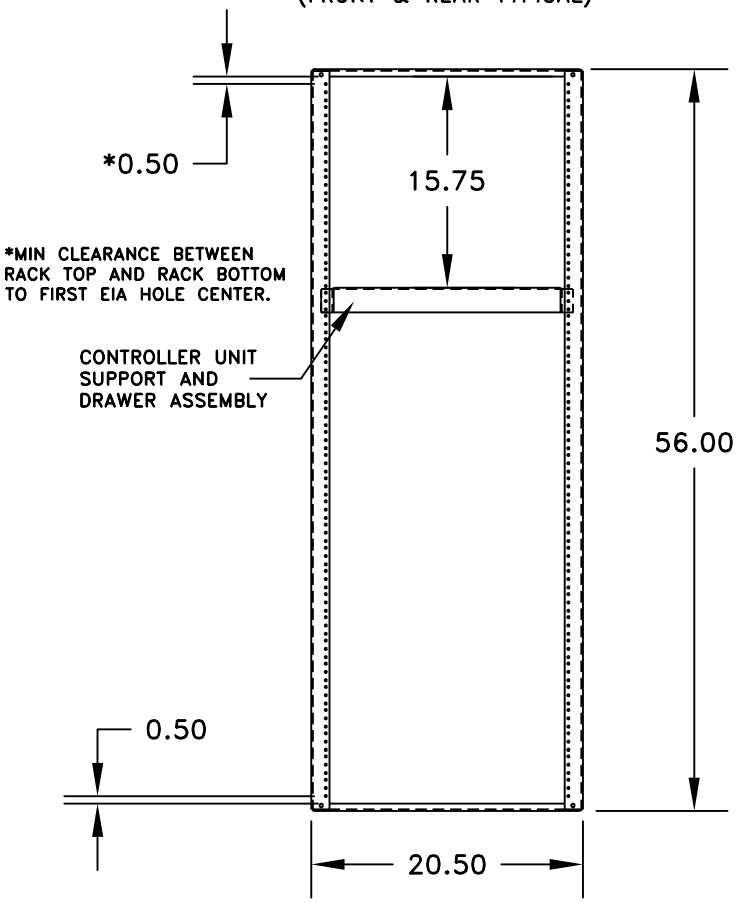
TITLE:

CABINET HOUSING #3
DETAIL 2

NO SCALE	
TEES, NOV 19, 1999	7-5-3

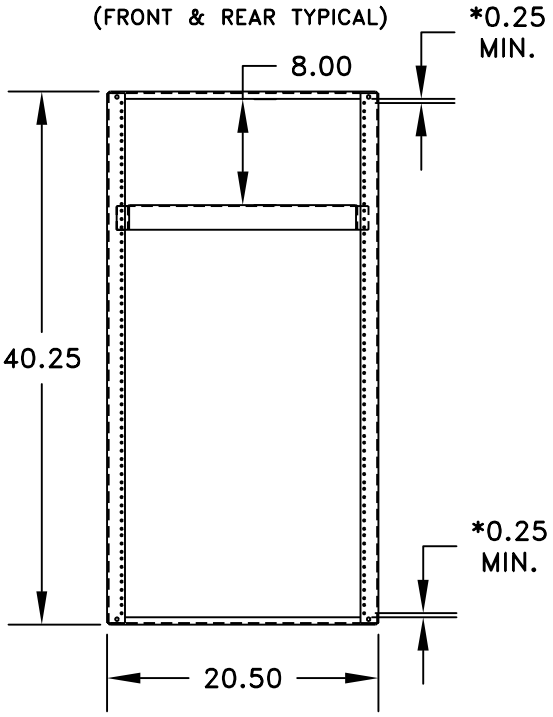
CAGE 1 DETAIL

FRONT VIEW
(FRONT & REAR TYPICAL)

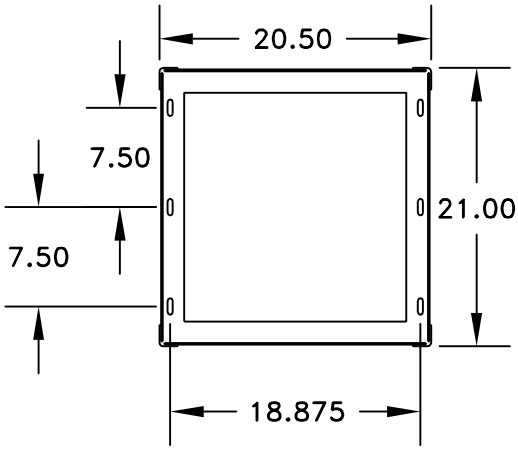


CAGE 2 DETAIL

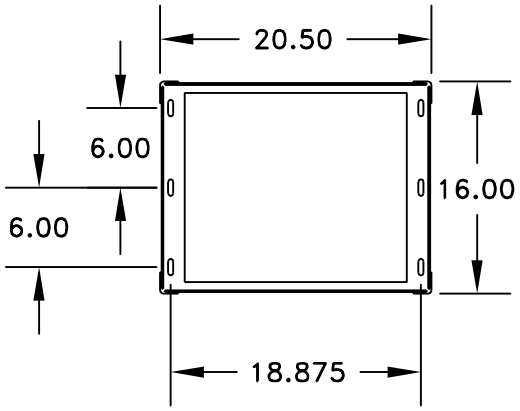
FRONT VIEW
(FRONT & REAR TYPICAL)



CAGE 1 TOP VIEW



CAGE 2 TOP VIEW

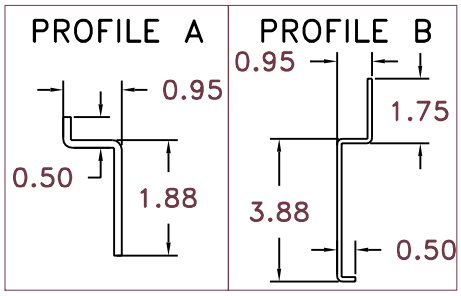


TITLE:

CABINET CAGES #1 & #2

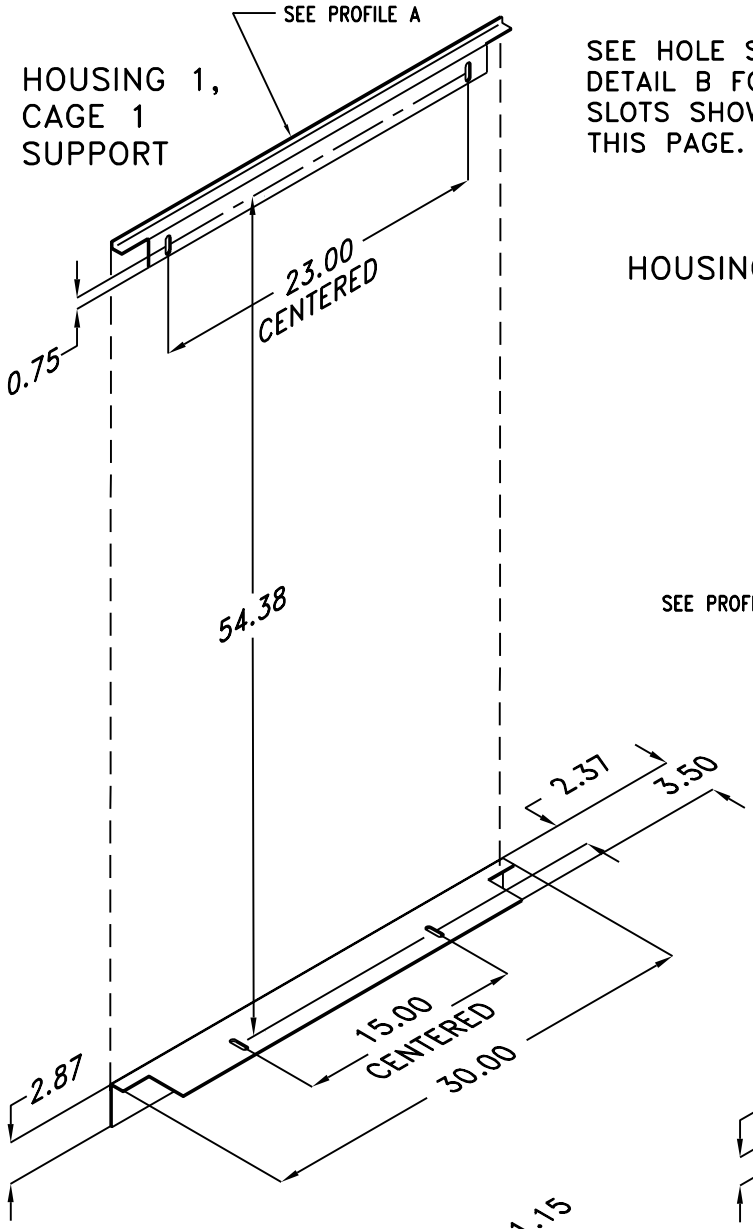
NO SCALE	
TEES, NOV 19, 1999	7-5-4

HOUSINGS 1 & 2 CAGE SUPPORT DETAILS

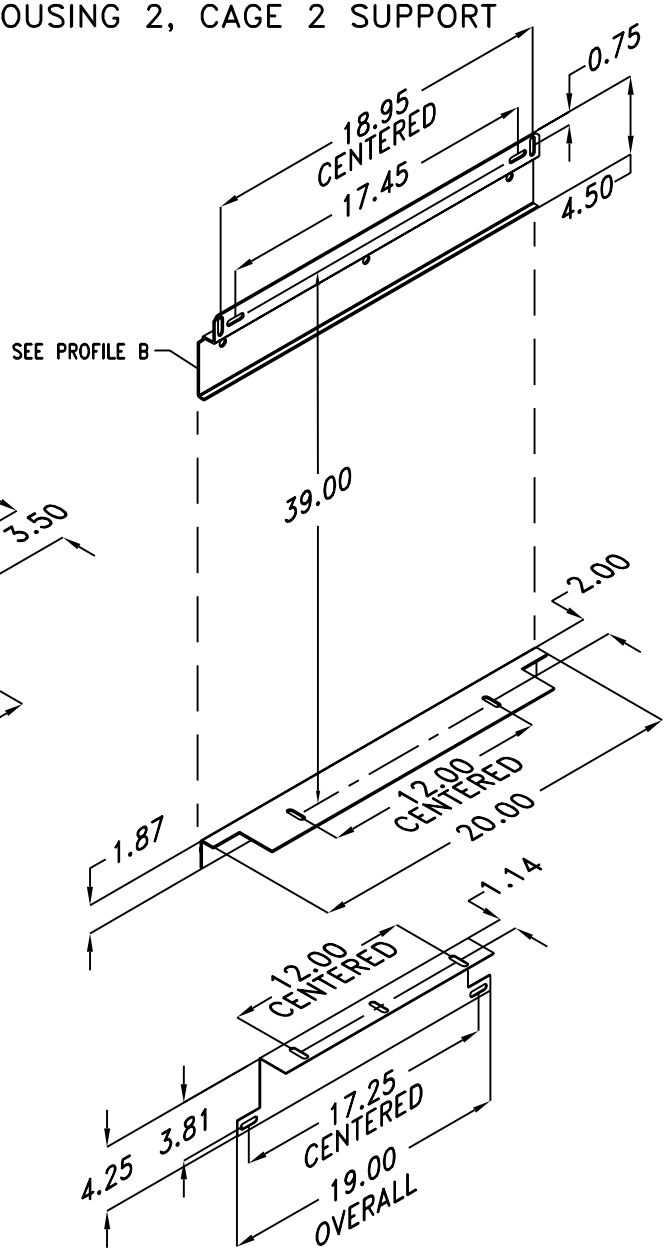


SEE HOLE SLOT DETAIL B FOR ALL SLOTS SHOWN ON THIS PAGE.

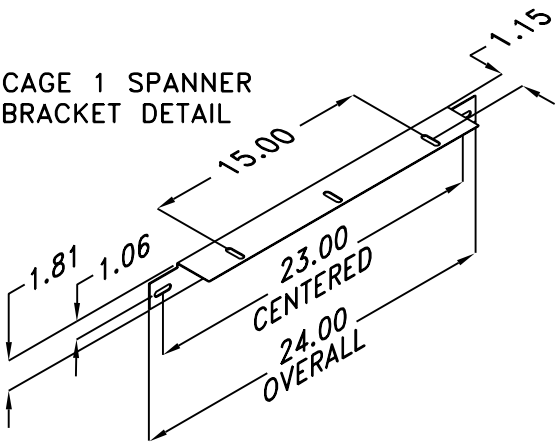
HOUSING 1, CAGE 1 SUPPORT



HOUSING 2, CAGE 2 SUPPORT



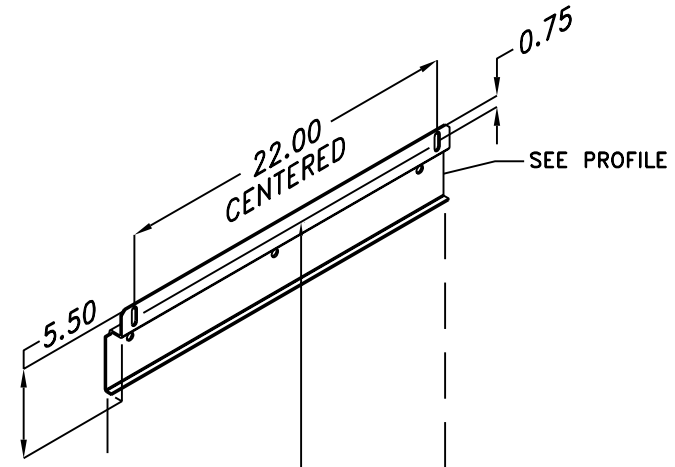
CAGE 1 SPANNER BRACKET DETAIL



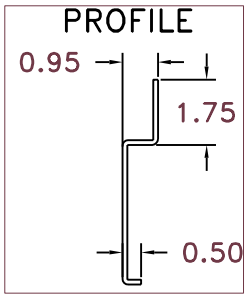
CAGE 2 SPANNER BRACKET DETAIL

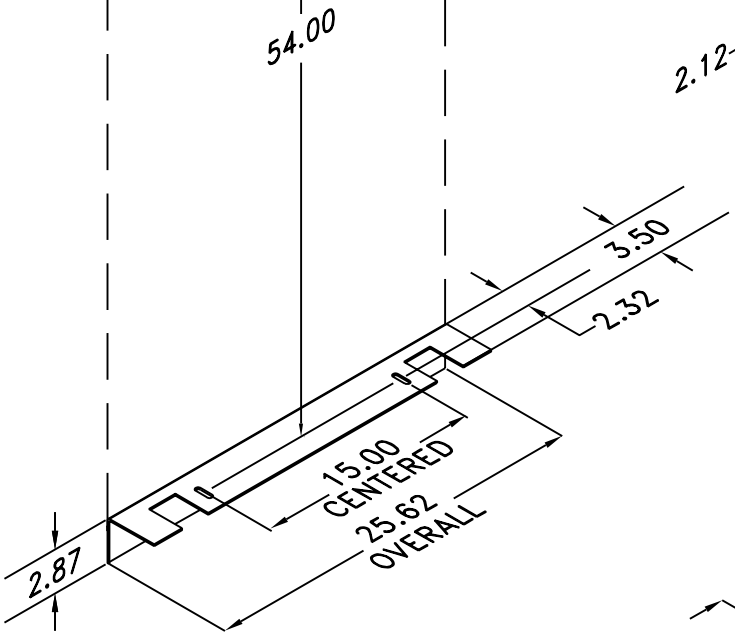
TITLE: CABINET CAGES TO HOUSING #1 & #2 SUPPORTS		
NO SCALE		
TEES, NOV 19, 1999		7-5-5

HOUSINGS 3 TO CAGE 1 SUPPORT DETAILS

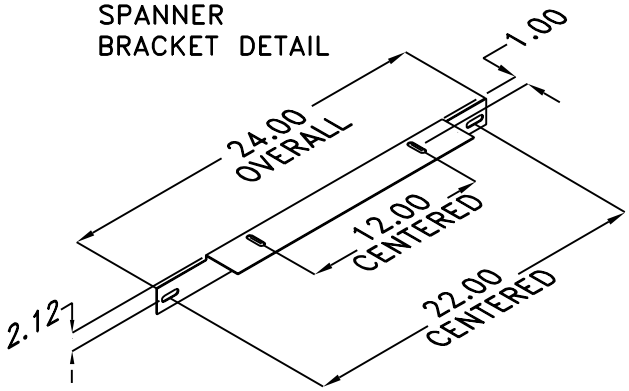


SEE HOLE SLOT DETAIL B FOR ALL SLOTS SHOWN ON THIS PAGE.

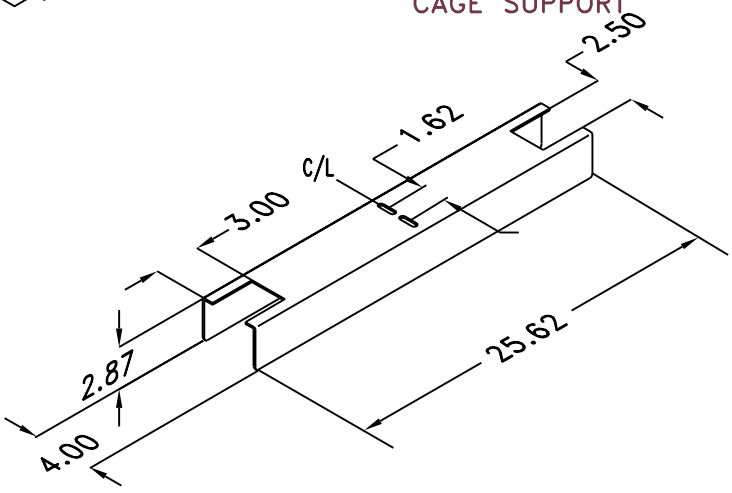




SPANNER BRACKET DETAIL



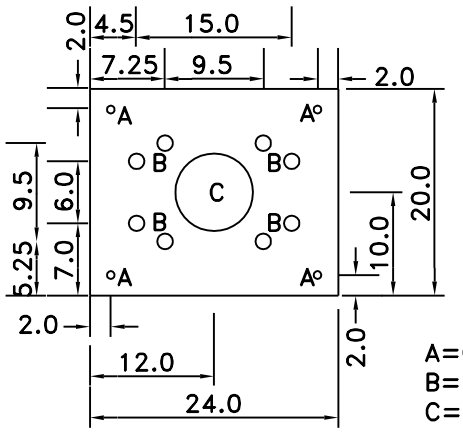
CENTER CHANNEL CAGE SUPPORT



TITLE: CABINET CAGE TO HOUSING #3 SUPPORT		
NO SCALE		
TEES, NOV 19, 1999		7-5-6

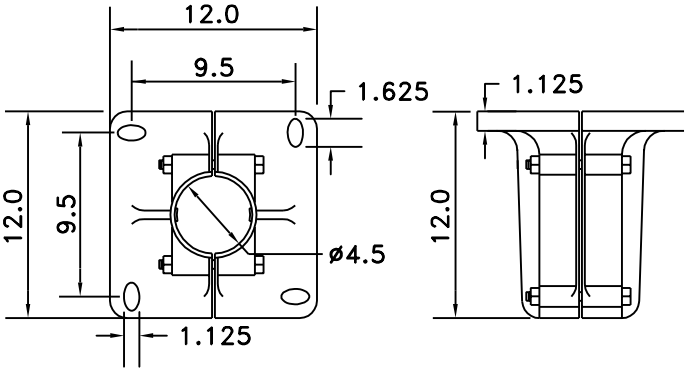
CABINET HOUSING 2 PEDESTAL ADAPTOR

SLIP FITTER BASE PLATE DETAIL (0.375 ALUMINUM)

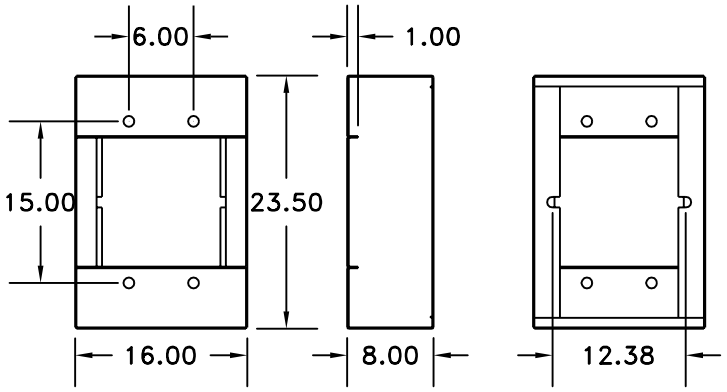


A=0.50 DIA.
B=1.00 DIA.
C=5.00 DIA.

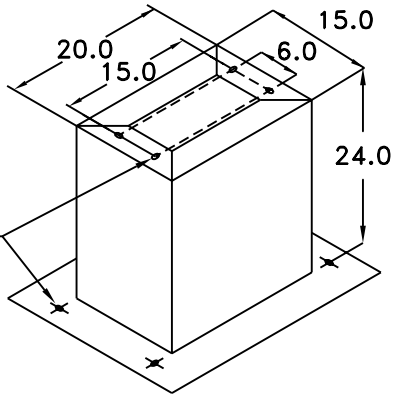
SLIP FITTER (CAST ALUMINUM) DETAIL

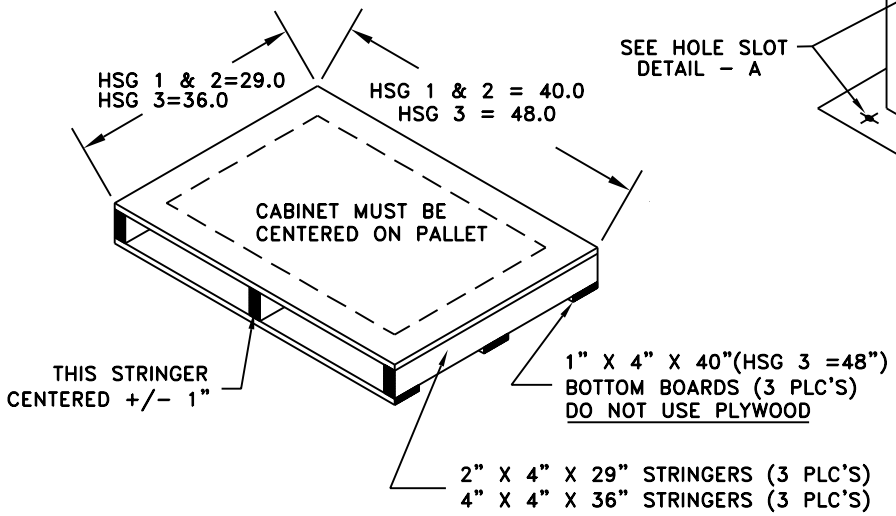


HOUSING 2 "M" STYLE BASE ADAPTER
NOTE: ALL HOLE PATTERNS ARE SYMMETRICALLY LOCATED.

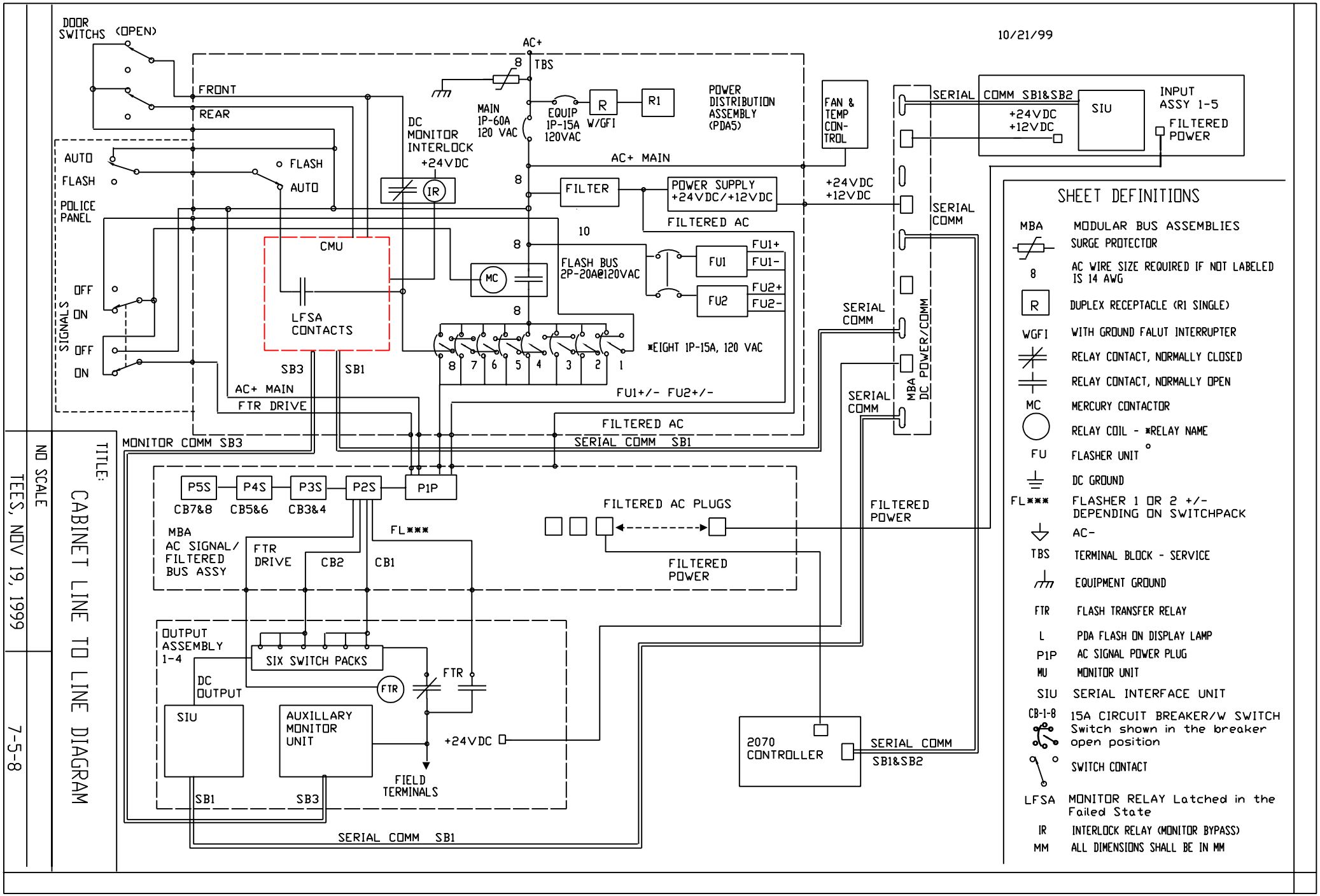


HOUSING 2 "P" STYLE BASE ADAPTER

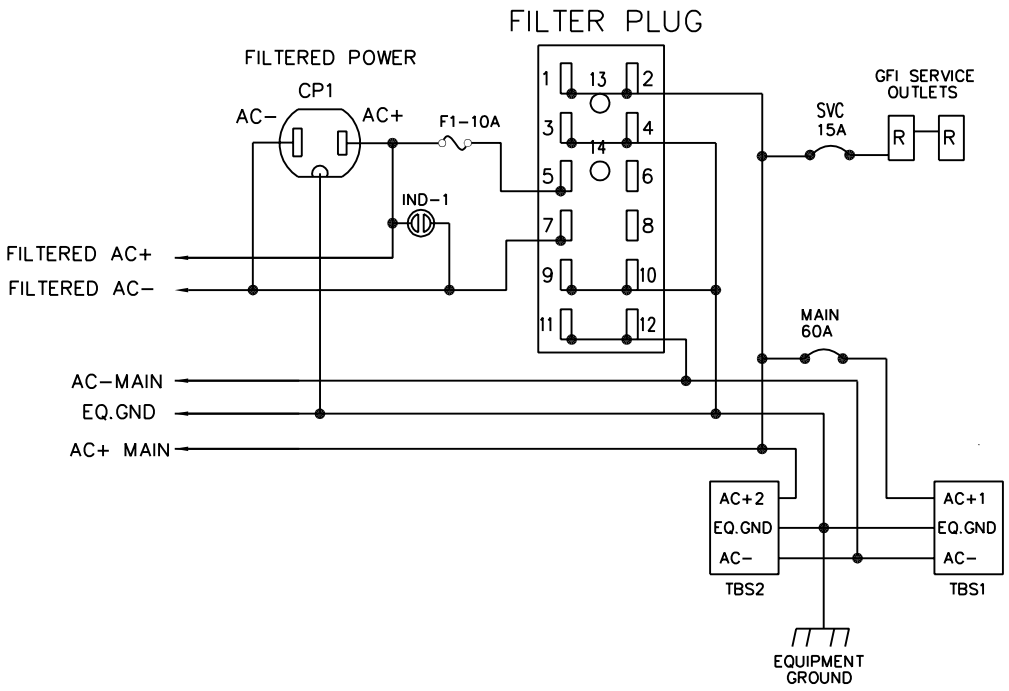




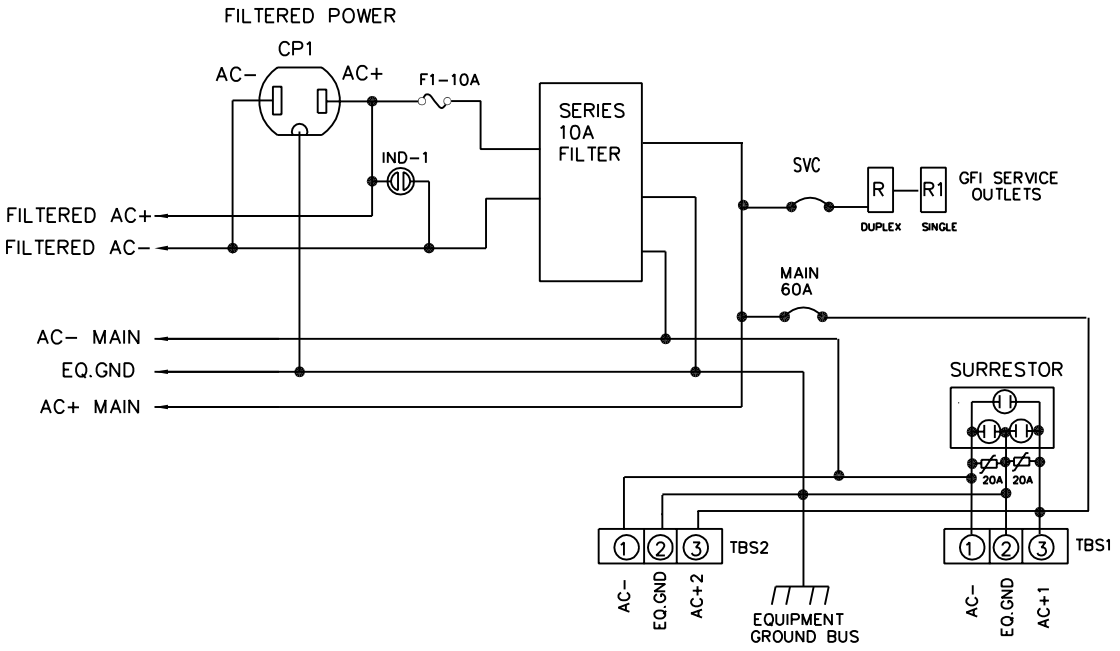
TITLE: CABINET ADAPTERS AND SHIPPING PLATFORMS	
NO SCALE	
TEES, NOV 19, 1999	7–5–7


DOOR SWITCHS (OPEN)
FRONT
REAR
AUTO
FLASH
POLICE PANEL
OFF
ON
OFF
ON
SIGNALS
CMU
LFSA CONTACTS
SB3
SB1
AC+ MAIN
FTR DRIVE
MONITOR COMM SB3
AC+
8
TBS
MAIN 1P-60A 120 VAC
EQUIP 1P-15A 120VAC
R
R1
W/GFI
POWER DISTRIBUTION ASSEMBLY (PDA5)
DC MONITOR INTERLOCK +24VDC
IR
AC+ MAIN
FILTER
POWER SUPPLY +24VDC/+12VDC
FILTERED AC
10
MC
FLASH BUS 2P-20A@120VAC
FU1
FU2
FU1+
FU1-
FU2+
FU2-
*EIGHT 1P-15A, 120 VAC
8 7 6 5 4 3 2 1
FU1+/- FU2+/-
FILTERED AC
SERIAL COMM SB1
FAN & TEMP CON-TROL
+24VDC +12VDC
SERIAL COMM
SERIAL COMM SB1&SB2
+24VDC +12VDC
SIU
INPUT ASSY 1-5
FILTERED POWER
SERIAL COMM
SERIAL COMM
MBA DC POWER/COMM
SERIAL COMM
P5S P4S P3S P2S P1P
CB7&8 CB5&6 CB3&4
MBA AC SIGNAL/ FILTERED BUS ASSY
FTR DRIVE
CB2
CB1
FL***
FILTERED AC PLUGS
FILTERED POWER
FILTERED POWER
OUTPUT ASSEMBLY 1-4
SIX SWITCH PACKS
DC OUTPUT
FTR
FTR
SIU
AUXILLARY MONITOR UNIT
+24VDC
FIELD TERMINALS
SB1
SB3
SERIAL COMM SB1
2070 CONTROLLER
SERIAL COMM SB1&SB2
10/21/99
SHEET DEFINITIONS
MBA MODULAR BUS ASSEMBLIES
SURGE PROTECTOR
8 AC WIRE SIZE REQUIRED IF NOT LABELED IS 14 AWG
R DUPLEX RECEPTACLE (R1 SINGLE)
WGFI WITH GROUND FALUT INTERRUPTER
RELAY CONTACT, NORMALLY CLOSED
RELAY CONTACT, NORMALLY OPEN
MC MERCURY CONTACTOR
RELAY COIL - *RELAY NAME
FU FLASHER UNIT
DC GROUND
FL*** FLASHER 1 OR 2 +/- DEPENDING ON SWITCHPACK
AC-
TBS TERMINAL BLOCK - SERVICE
EQUIPMENT GROUND
FTR FLASH TRANSFER RELAY
L PDA FLASH ON DISPLAY LAMP
P1P AC SIGNAL POWER PLUG
MU MONITOR UNIT
SIU SERIAL INTERFACE UNIT
CB-1-8 15A CIRCUIT BREAKER/W SWITCH
Switch shown in the breaker open position
SWITCH CONTACT
LFSA MONITOR RELAY Latched in the Failed State
IR INTERLOCK RELAY (MONITOR BYPASS)
MM ALL DIMENSIONS SHALL BE IN MM
TITLE:
CABINET LINE TO LINE DIAGRAM
NO SCALE
TEES, NOV 19, 1999
7-5-8

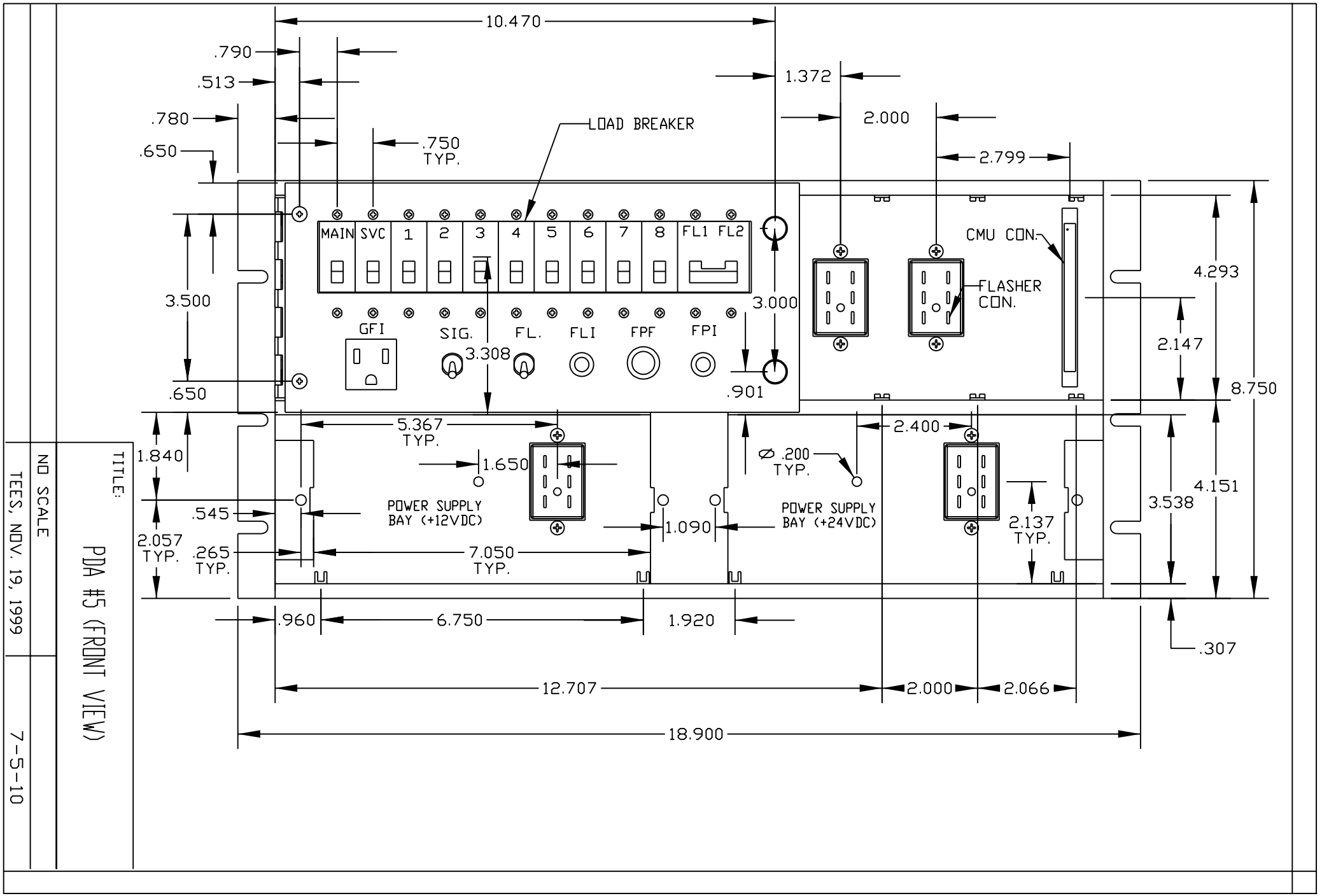
OPTIONAL PLUGGABLE FILTER ASSEMBLY



FIXED FILTER ASSEMBLY



	TITLE: CABINET POWER PROTECTION AND FILTERING	
	NO SCALE	
	TEES, NOV 19, 1999	7–5–9



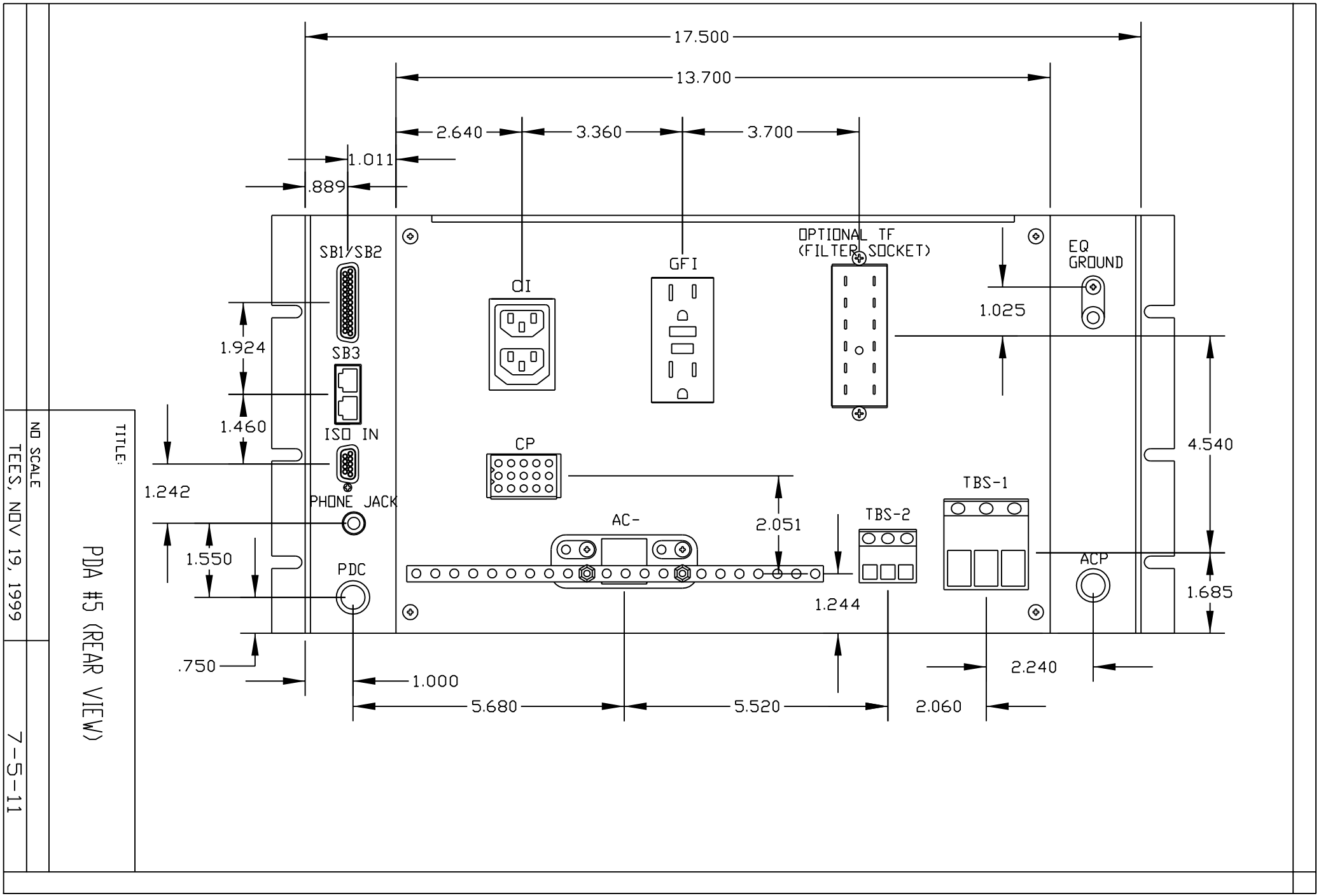
TITLE:

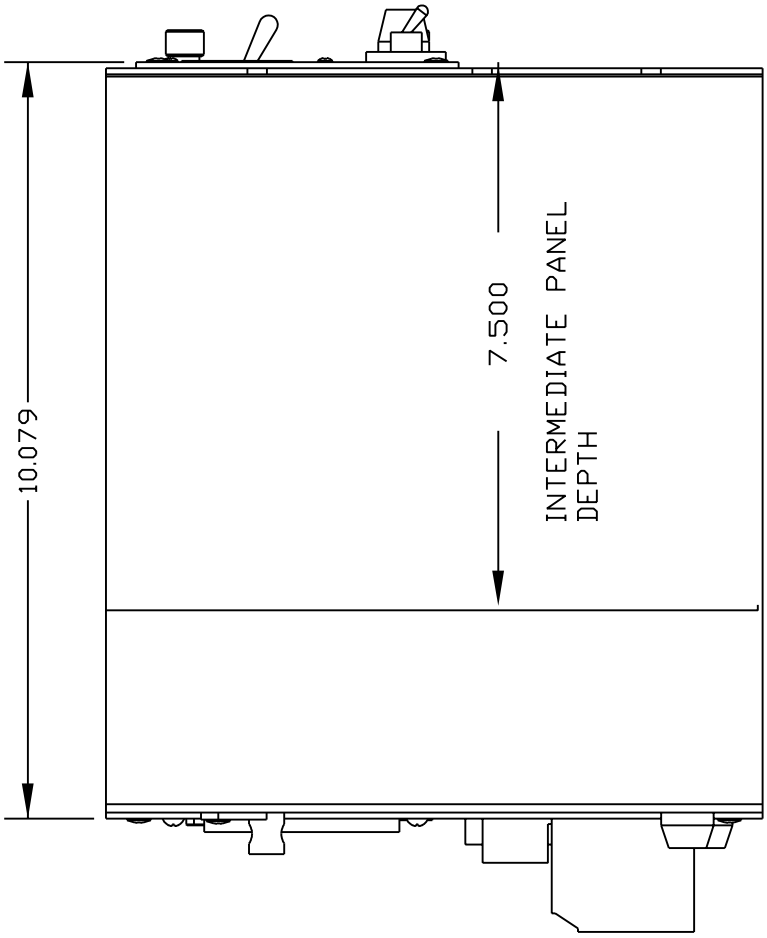
PDA #5 (FRONT VIEW)

NO SCALE

TEES, NOV. 19, 1999

7-5-10


17.500
13.700
2.640
3.360
3.700
1.011
.889
SB1/SB2
SB3
ISO IN
PHONE JACK
PDC
CI
GFI
OPTIONAL TF
(FILTER SOCKET)
EQ
GROUND
CP
AC-
TBS-1
TBS-2
ACP
1.924
1.460
1.242
1.550
1.025
2.051
1.244
4.540
1.685
.750
1.000
5.680
5.520
2.240
2.060
TITLE:
PDA #5 (REAR VIEW)
NO SCALE
TEES, NOV 19, 1999
7-5-11



TITLE:

PDA #5 (SIDE VIEW)

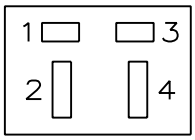
NO SCALE

TEES, NOV 19, 1999

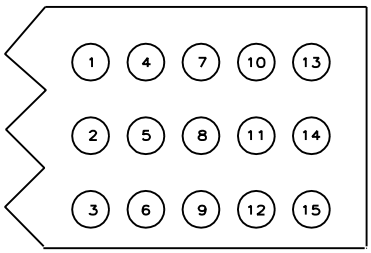
7-5-12

PDA #5 CONNECTORS and PIN ASSIGNMENTS

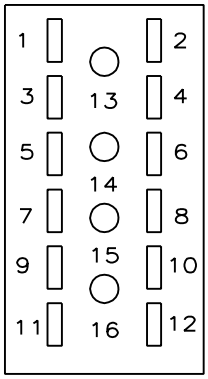
PDC (Plug)



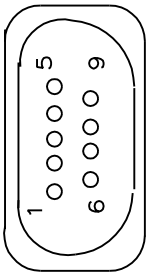
CC (Socket)



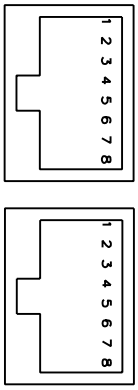
ACSIGNAL POWER P(Plug)



CDC (Socket)

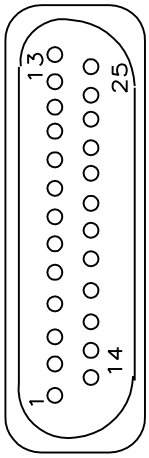


SB3 (Sockets)

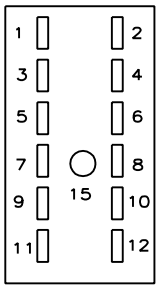


SB3 SOCKETS WIRED IN PARALLEL FOR DAISY-CHAIN

SB1/SB2 (Socket)



OPTIONAL TF (FILTER SOCKET)



MONITOR RESET TEST PLUG AND RECEPTACLE

MONITOR RESET (Ring)

PDA MONITOR RESET (Tip)

CC (Cabinet) CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
CC-1	MC COIL (To Police Panel)	CC-2	AC+MAIN (To Police Panel)
CC-3	AC+ (To FTR Coils)	CC-4	AC+MAIN (Front Door Sw.)
CC-5	FRONT DOOR SWITCH (NC)	CC-6	POLICE FLASH SWITCH
CC-7	AC+MAIN (Rear Door Sw.)	CC-8	REAR DOOR SWITCH (NC)
CC-9		CC-10	AC SIGNAL BREAKERS
CC-11		CC-12	
CC-13	IA & MCE COMMON	CC-14	MCE (Man Cont Enable)SW.
CC-15	IA (Interval Advance)SWITCH		

AC SIGNAL POWER CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
P-1	LB1 AC+	P-2	LB2 AC+
P-3	LB3 AC+	P-4	LB4 AC+
P-5	LB5 AC+	P-6	LB6 AC+
P-7	LB7 AC+	P-8	LB8 AC+
P-9	FL1+	P-10	FL1-
P-11	FL2+	P-12	FL2-
P-13	EQ. GROUND	P-14	FTR COIL DRIVE
P-15	AC+ MAIN	P-16	AC- MAIN

SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE PDA	Pin	AT THE CONTROLLER	AT THE PDA
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD-	SB1 RXD-
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD-	SB1 TXD-
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC-	SB1 RXC-
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC-	SB1 TXC-
5	SB2 TXD+	NC	18	SB2 TXD-	NC
6	SB2 RXD+	NC	19	SB2 RXD-	NC
7	SB2 TXC+	NC	20	SB2 TXC-	NC
8	SB2 RXC+	NC	21	SB2 RXC-	NC
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC-	LINE SYNC-
10	NRESET+	NRESET+	23	NRESET-	NRESET-
11	PWR DWN+	PWR DWN+	24	PWR DWN-	PWR DWN-
12	+5VDC ISO	+5VDC ISO	25	EQ GND	EQ GND
13	DC GND#2	DC GND#2			

TF(FILTER) CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
TF-1	AC+ MAIN	TF-2	AC+ MAIN
TF-3	EQ. GROUND	TF-4	EQ. GROUND
TF-5	AC+ FILTERED POWER	TF-6	DRY CONTACT 1
TF-7	AC- FILTERED POWER	TF-8	DRY CONTACT 2
TF-9	EQ. GROUND	TF-10	EQ. GROUND
TF-11	AC- MAIN	TF-12	AC- MAIN

PDC (DC Power) CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
PDC 1	+24VDC	PDC 3	+12VDC
PDC 2	DC GROUND	PDC 4	DC GROUND

CDC (Cabinet DC signal interconnect)

Pin #	FUNCTION	Pin #	FUNCTION
CDC-1	MCE (Manual Control Enable)	CDC-2	IA (Interval Advance)
CDC-3	TPS (Transient Prot. Status)	CDC-4	Spare
CDC-5	MCE,IA,TPS Common	CDC-6	Spare
CDC-7	Spare	CDC-8	EXTERNAL RESET**
CDC-9	DC GROUND		

**EXTERNAL RESET Signal must go through a Phone Plug. This signal is to be used only during diagnostic testing.

SB3 CONNECTOR

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SP3 TXC+	SP3 RXC+
2	ORANGE	SP3 TXC-	SP3 RXC-
3	WHITE GREEN	DC GROUND	DC GROUND
4	BLUE	SP3 TXD+	SP3 RXD+
5	WHITE BLUE	SP3 TXD-	SP3 RXD-
6	GREEN	DC GROUND	DC GROUND
7	WHITE BROWN	SP3 RXD+	SP3 TXD+
8	BROWN	SP3 RXD-	SP3 TXD-

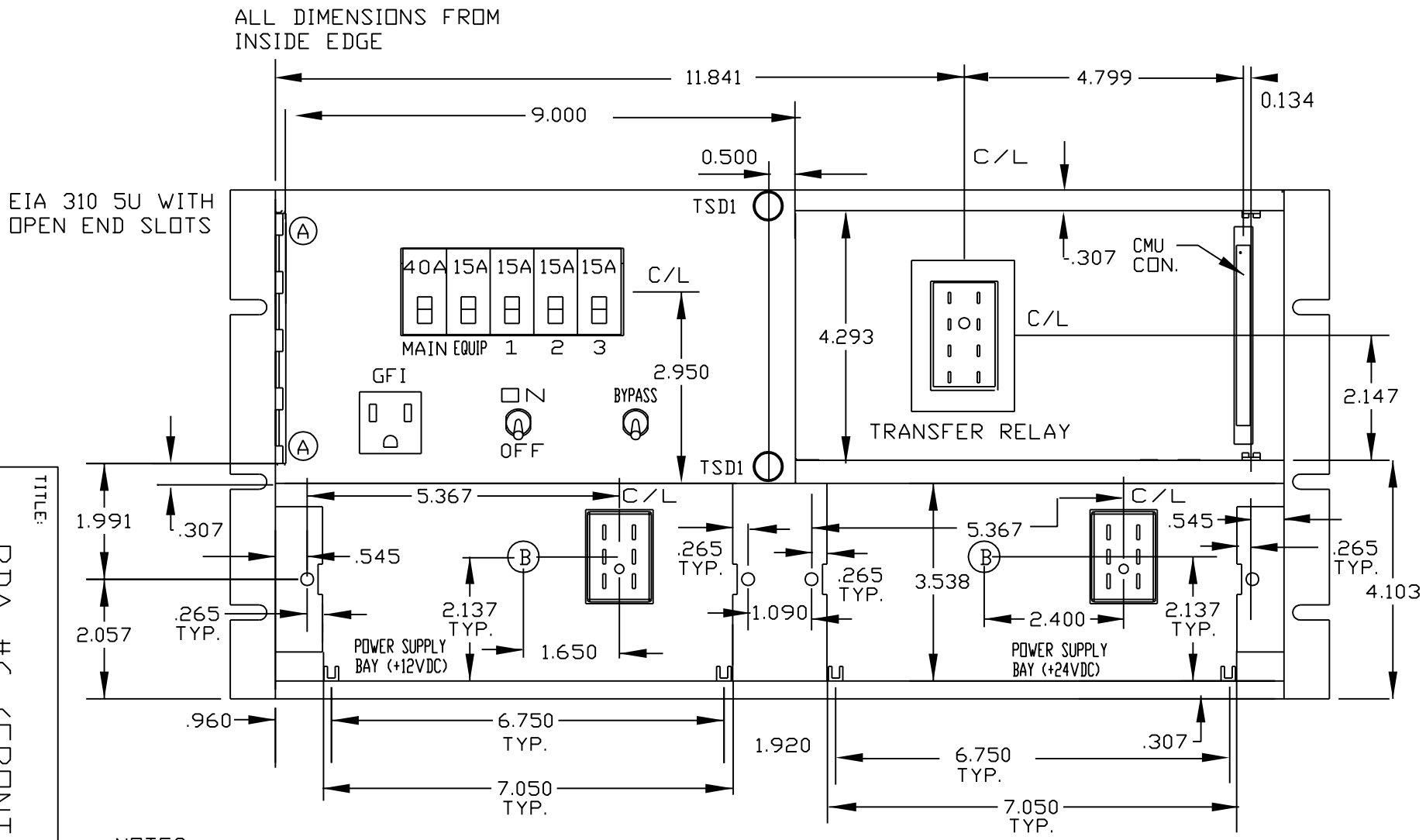
TITLE:

PDA 5 CONNECTORS and PIN ASSIGNMENTS

NO SCALE

TEES, NOV 19, 1999

7-5-13



NOTES:

1. ALL DIMENSIONS IN INCHES
2. O PEM NUT FOR TSD1 DEVICE (4 PLACES)
3. (A) PIANO HINGE FASTNER (2PLACES)
4. (B) CLEAR 8:32 STUD (TWO PLACES)
5. ALL ITEMS SHALL BE A MINIMUM OF 1.5 INCHES CENTER TO CENTER EXCEPT FOR CIRCUIT BREAKERS

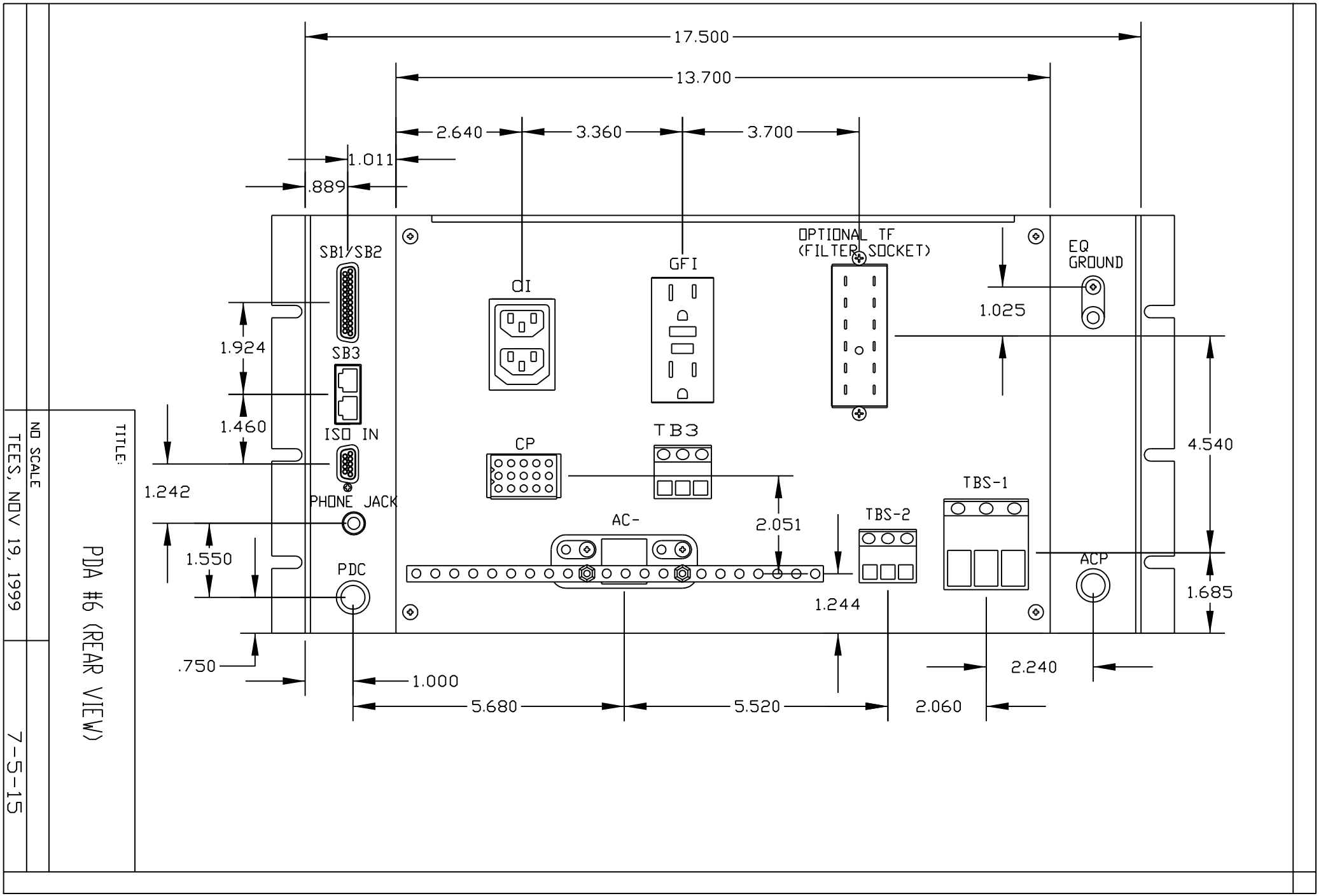
TITLE:

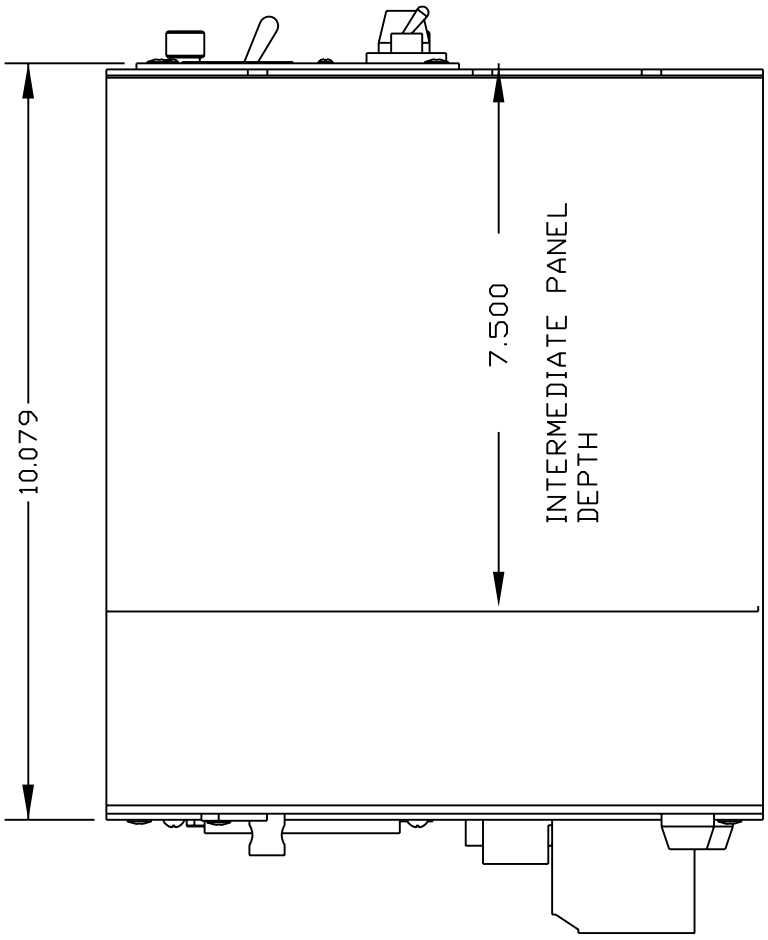
PDA #6 (FRONT VIEW)

NO SCALE

TEES, NOV 19, 1999

7-5-14

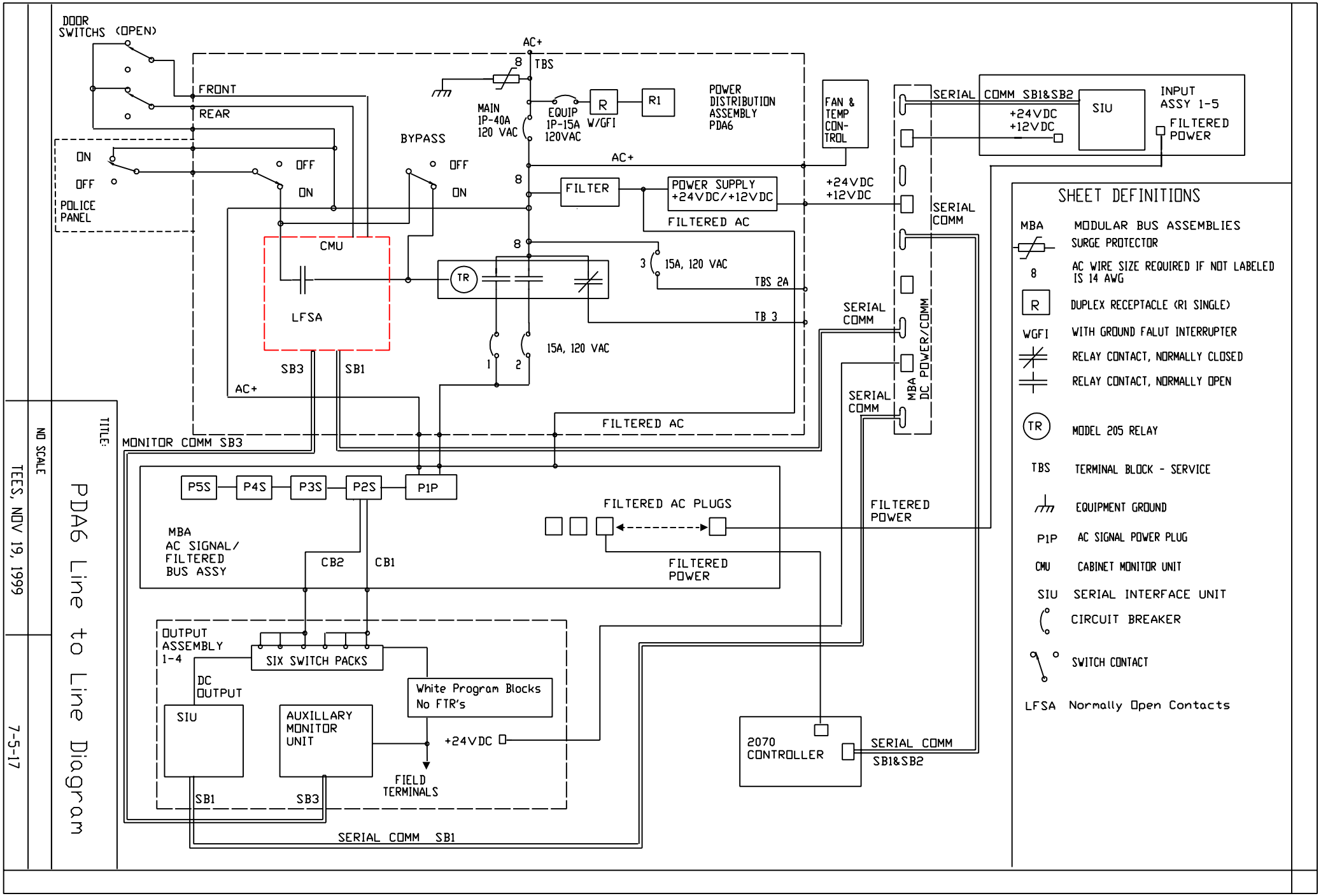

17.500
13.700
2.640
3.360
3.700
1.011
.889
SB1/SB2
SB3
ISO IN
PHONE JACK
PDC
CI
GFI
OPTIONAL TF
(FILTER SOCKET)
EQ
GROUND
1.025
1.924
1.460
1.242
1.550
CP
TB3
AC-
2.051
TBS-2
TBS-1
ACP
4.540
1.685
1.244
.750
1.000
5.680
5.520
2.060
2.240
TITLE:
PDA #6 (REAR VIEW)
NO SCALE
TEES, NOV 19, 1999
7-5-15

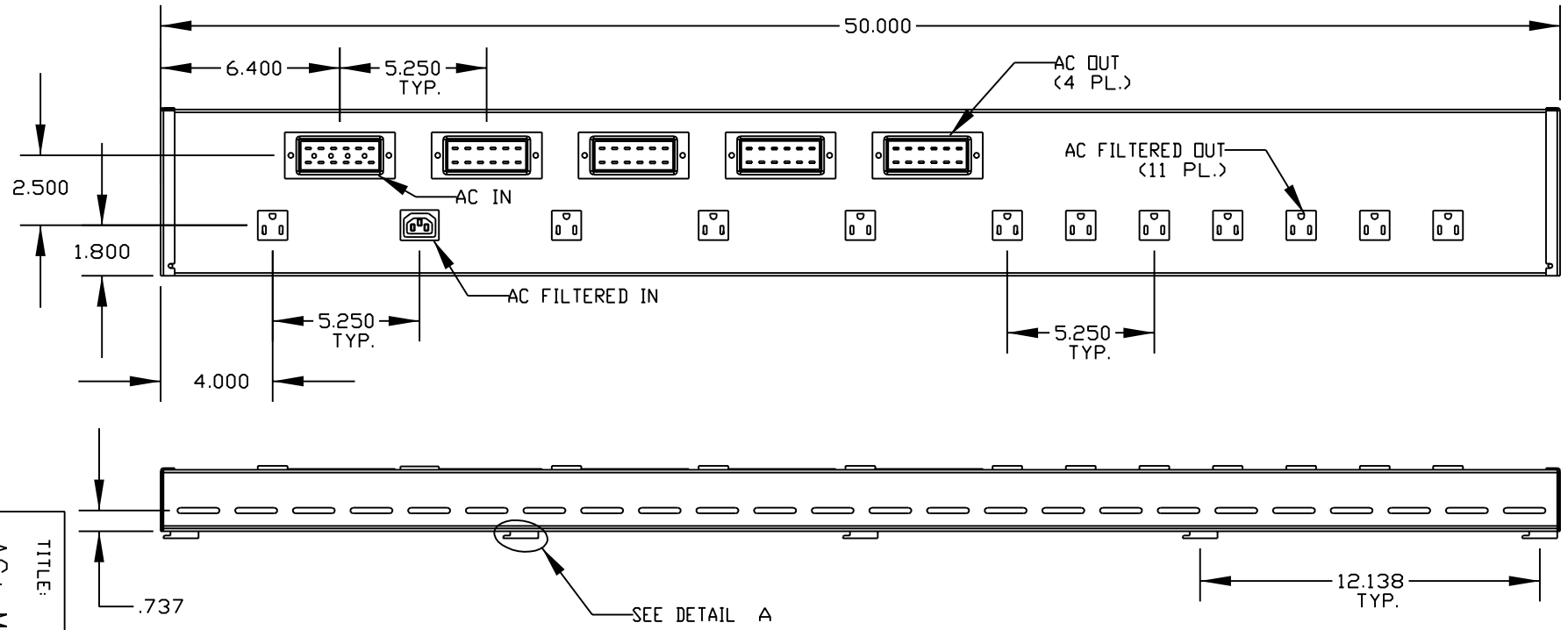


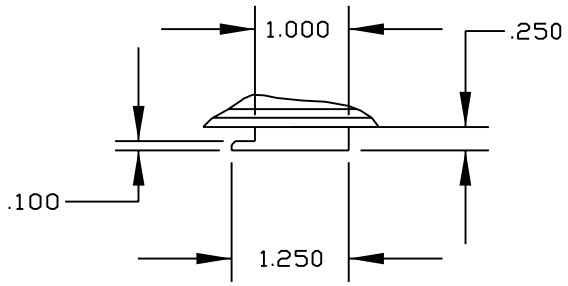
TITLE:

PDA #6 (SIDE VIEW)

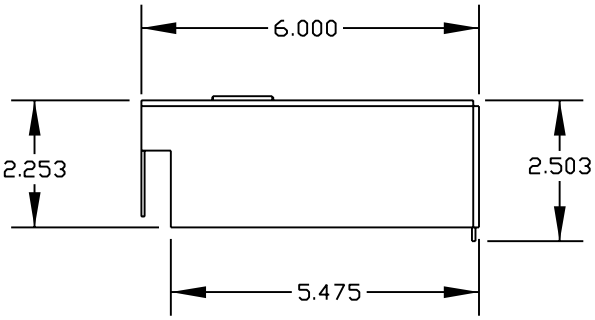
	NO SCALE	
	TEES, NOV 19, 1999	7-5-16


DOOR SWITCHS (OPEN)
FRONT
REAR
ON
OFF
POLICE PANEL
BYPASS
OFF
ON
AC+
8
TBS
MAIN 1P-40A 120 VAC
EQUIP 1P-15A 120VAC
R
W/GFI
R1
POWER DISTRIBUTION ASSEMBLY PDA6
FAN & TEMP CON-TROL
FILTER
POWER SUPPLY +24VDC/+12VDC
+24VDC +12VDC
FILTERED AC
CMU
LFSA
TR
3
15A, 120 VAC
TBS 2A
TB 3
1
2
15A, 120 VAC
SB3
SB1
AC+
FILTERED AC
SERIAL COMM
MBA DC POWER/COMM
SERIAL COMM SB1&SB2
+24VDC +12VDC
SIU
INPUT ASSY 1-5
FILTERED POWER
MONITOR COMM SB3
P5S
P4S
P3S
P2S
P1P
MBA AC SIGNAL/ FILTERED BUS ASSY
CB2
CB1
FILTERED AC PLUGS
FILTERED POWER
OUTPUT ASSEMBLY 1-4
SIX SWITCH PACKS
DC OUTPUT
SIU
AUXILLARY MONITOR UNIT
White Program Blocks No FTR's
+24VDC
FIELD TERMINALS
SB1
SB3
SERIAL COMM SB1
2070 CONTROLLER
SERIAL COMM SB1&SB2
SHEET DEFINITIONS
MBA MODULAR BUS ASSEMBLIES
SURGE PROTECTOR
8 AC WIRE SIZE REQUIRED IF NOT LABELED IS 14 AWG
R DUPLEX RECEPTACLE (R1 SINGLE)
WGFI WITH GROUND FALUT INTERRUPTER
RELAY CONTACT, NORMALLY CLOSED
RELAY CONTACT, NORMALLY OPEN
TR MODEL 205 RELAY
TBS TERMINAL BLOCK - SERVICE
EQUIPMENT GROUND
P1P AC SIGNAL POWER PLUG
CMU CABINET MONITOR UNIT
SIU SERIAL INTERFACE UNIT
CIRCUIT BREAKER
SWITCH CONTACT
LFSA Normally Open Contacts
TITLE:
PDA6 Line to Line Diagram
NO SCALE
TEES, NOV 19, 1999
7-5-17





DETAIL A



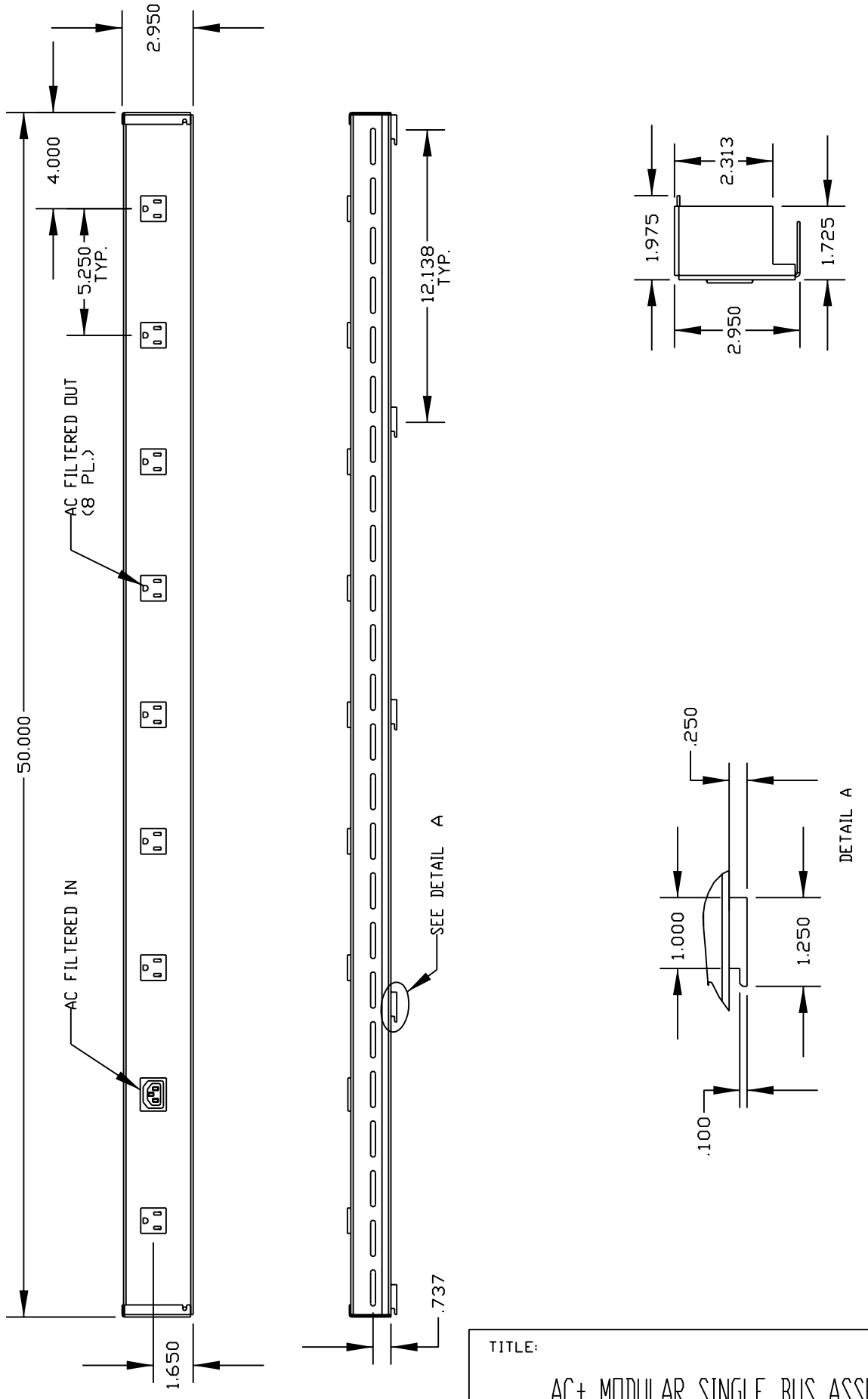
TITLE:

AC+ MODULAR DUAL BUS ASSEMBLY

NO SCALE

TEES, NOV 19, 1999

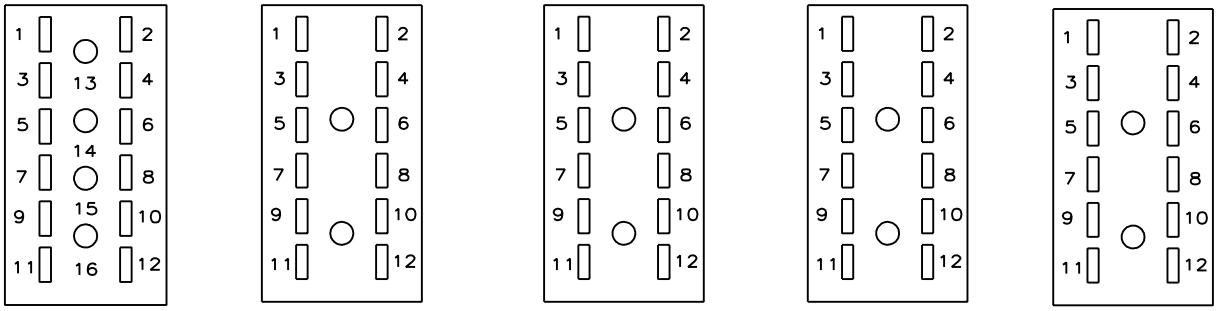
7-5-18



TITLE:

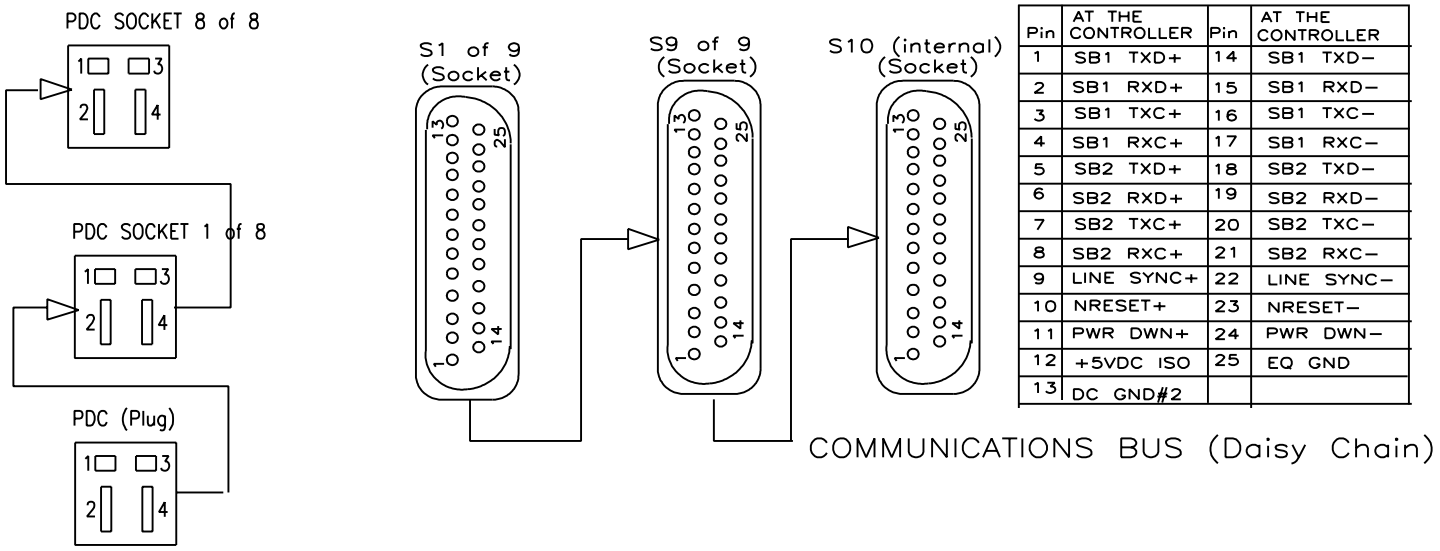
AC+ MODULAR SINGLE BUS ASSEMBLY

NO SCALE	
TEES, NOV 19, 1999	7-5-19



AC SIGNAL POWER BUS

Pin	P1 INPUT AC	Pin	S4 OUTPUT ASSY 4	Pin	S3 OUTPUT ASSY 3		S2 OUTPUT ASSY 2		S1 OUTPUT ASSY 1
1	LB1 AC+	1	LB7 AC+	1	LB5 AC+	1	LB3 AC+	1	LB1 AC+
2	LB2 AC+	2	LB8 AC+	2	LB6 AC+	2	LB4 AC+	2	LB2 AC+
3	LB3 AC+	3	FL1 −	3	FL1 +	3	FL1 −	3	FL1 +
4	LB4 AC+	4	FL1+	4	FL1−	4	FL1+	4	FL1−
5	LB5 AC+	5	FL2−	5	FL2+	5	FL2−	5	FL2+
6	LB6 AC+	6	FL2+	6	FL2−	6	FL2+	6	FL2−
7	LB7 AC+	7	FTR COIL DRIVE	7	FTR COIL DRIVE	7	FTR COIL DRIVE	7	FTR COIL DRIVE
8	LB8 AC+	8	AC+ MAIN	8	AC+ MAIN	8	AC+ MAIN	8	AC+ MAIN
9	FL1 +	9	AC− MAIN	9	AC− MAIN	9	AC− MAIN	9	AC− MAIN
10	FL1−	10	AC− MAIN	10	AC− MAIN	10	AC− MAIN	10	AC− MAIN
11	FL2+	11	EQ. GROUND	11	EQ. GROUND	11	EQ. GROUND	11	EQ. GROUND
12	FL2−	12	EQ. GROUND	12	EQ. GROUND	12	EQ. GROUND	12	EQ. GROUND
13	EQ. GROUND								
14	FTR COIL DRIVE								
15	AC+ MAIN								
16	AC− MAIN								



Pin	AT THE CONTROLLER	Pin	AT THE CONTROLLER
1	SB1 TXD+	14	SB1 TXD−
2	SB1 RXD+	15	SB1 RXD−
3	SB1 TXC+	16	SB1 TXC−
4	SB1 RXC+	17	SB1 RXC−
5	SB2 TXD+	18	SB2 TXD−
6	SB2 RXD+	19	SB2 RXD−
7	SB2 TXC+	20	SB2 TXC−
8	SB2 RXC+	21	SB2 RXC−
9	LINE SYNC+	22	LINE SYNC−
10	NRESET+	23	NRESET−
11	PWR DWN+	24	PWR DWN−
12	+5VDC ISO	25	EQ GND
13	DC GND#2		

PDC (DC Power) CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
PDC 1	+24VDC	PDC 3	+12VDC
PDC 2	DC GROUND	PDC 4	DC GROUND

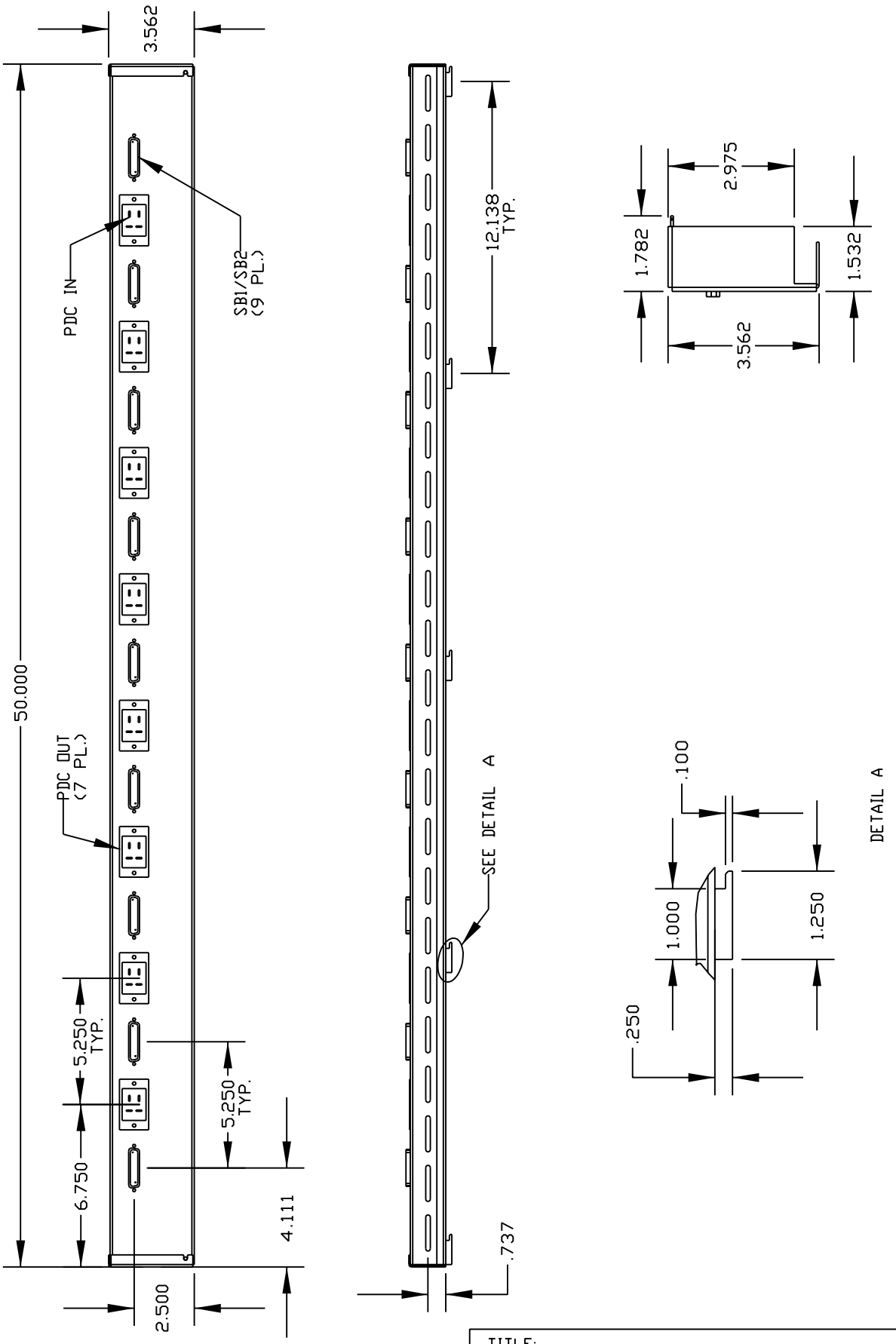
TITLE:

AC+ MODULAR BUS ASSEMBLY
POWER CONNETORS

NO SCALE

TEES, NOV 19, 1999

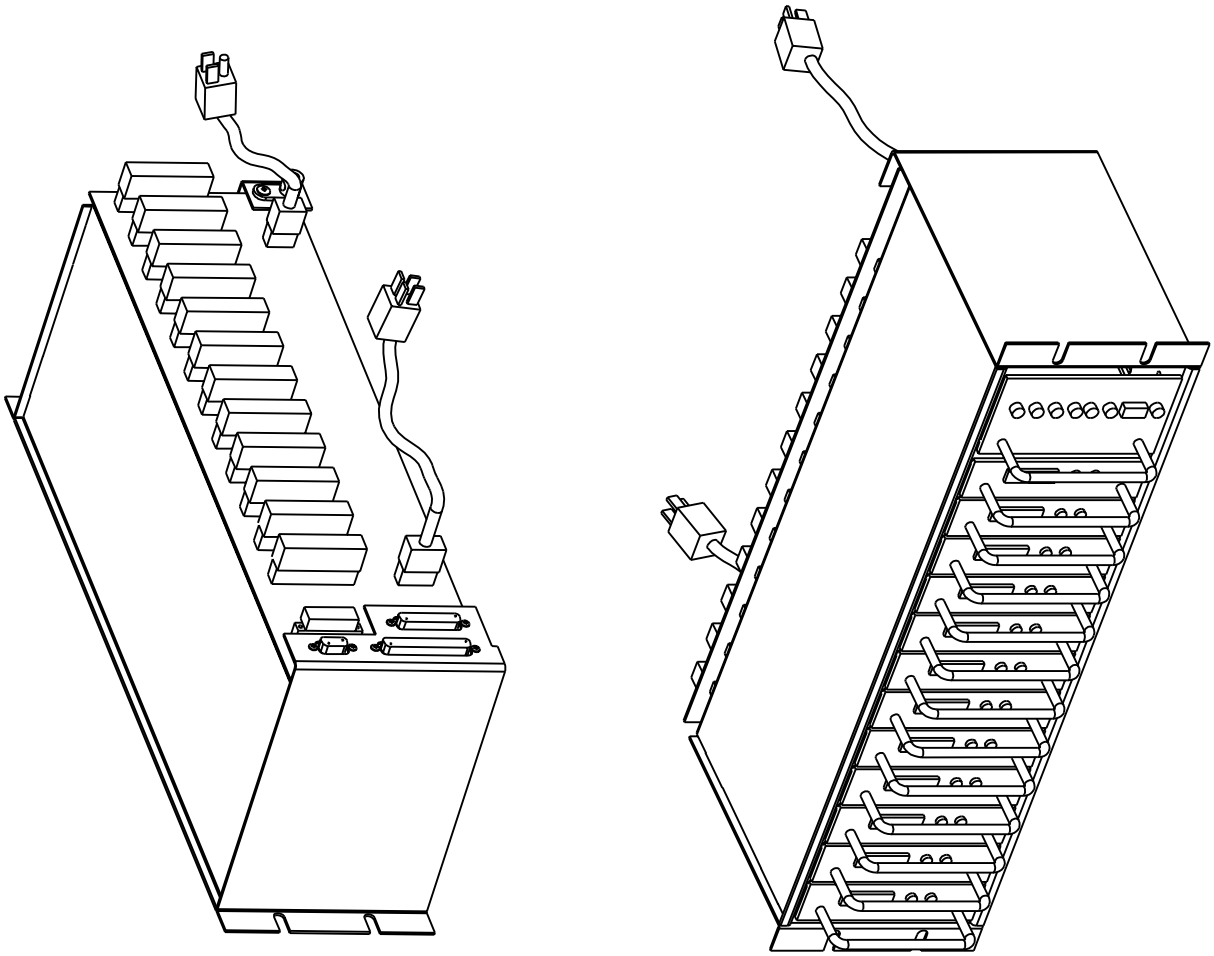
7−5−20



TITLE:

COMMUNICATIONS & DC POWER MODULAR BUS ASSEMBLY

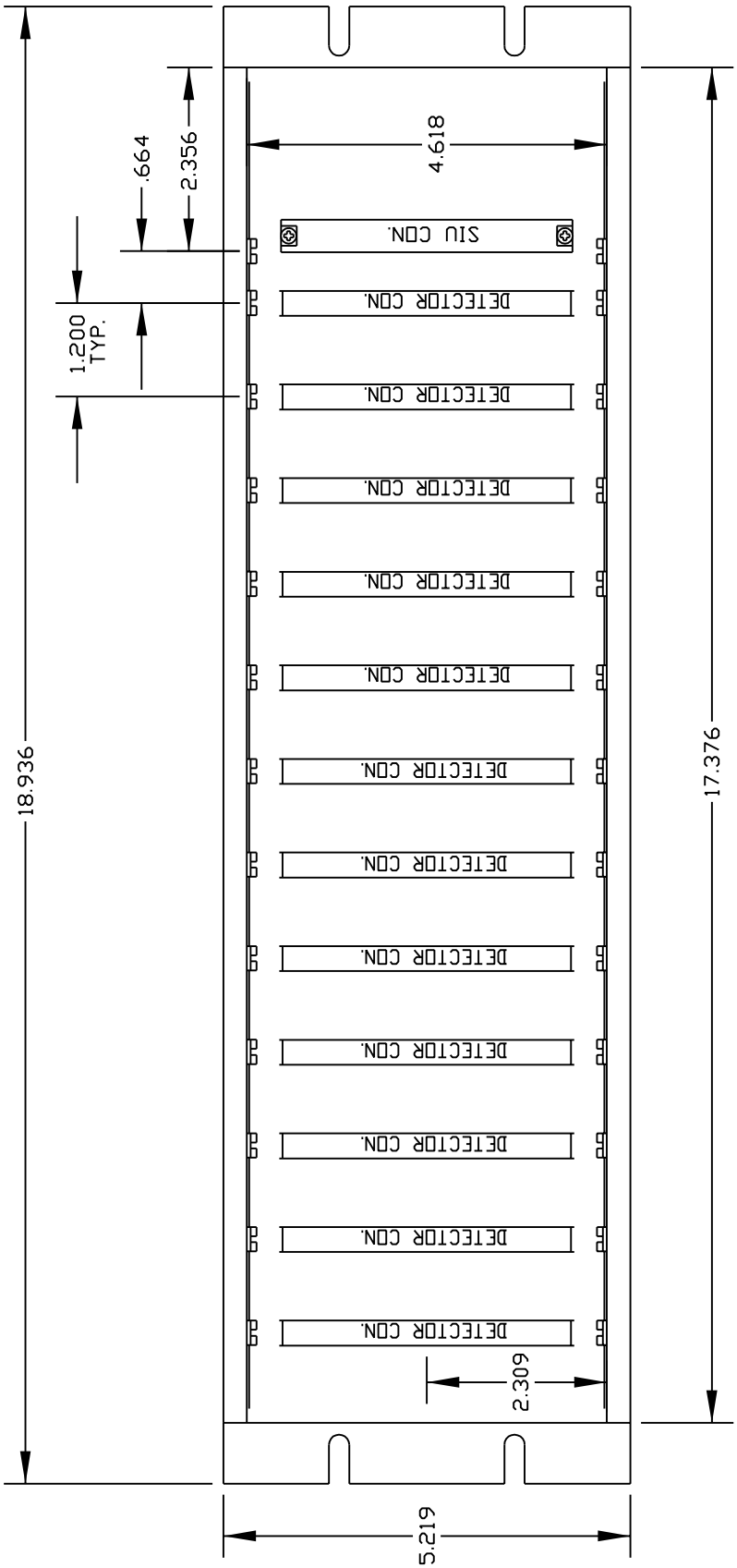
NO SCALE	
TEES, NOV 19, 1999	7-5-21



TITLE:

INPUT ASSEMBLY (DETAIL)

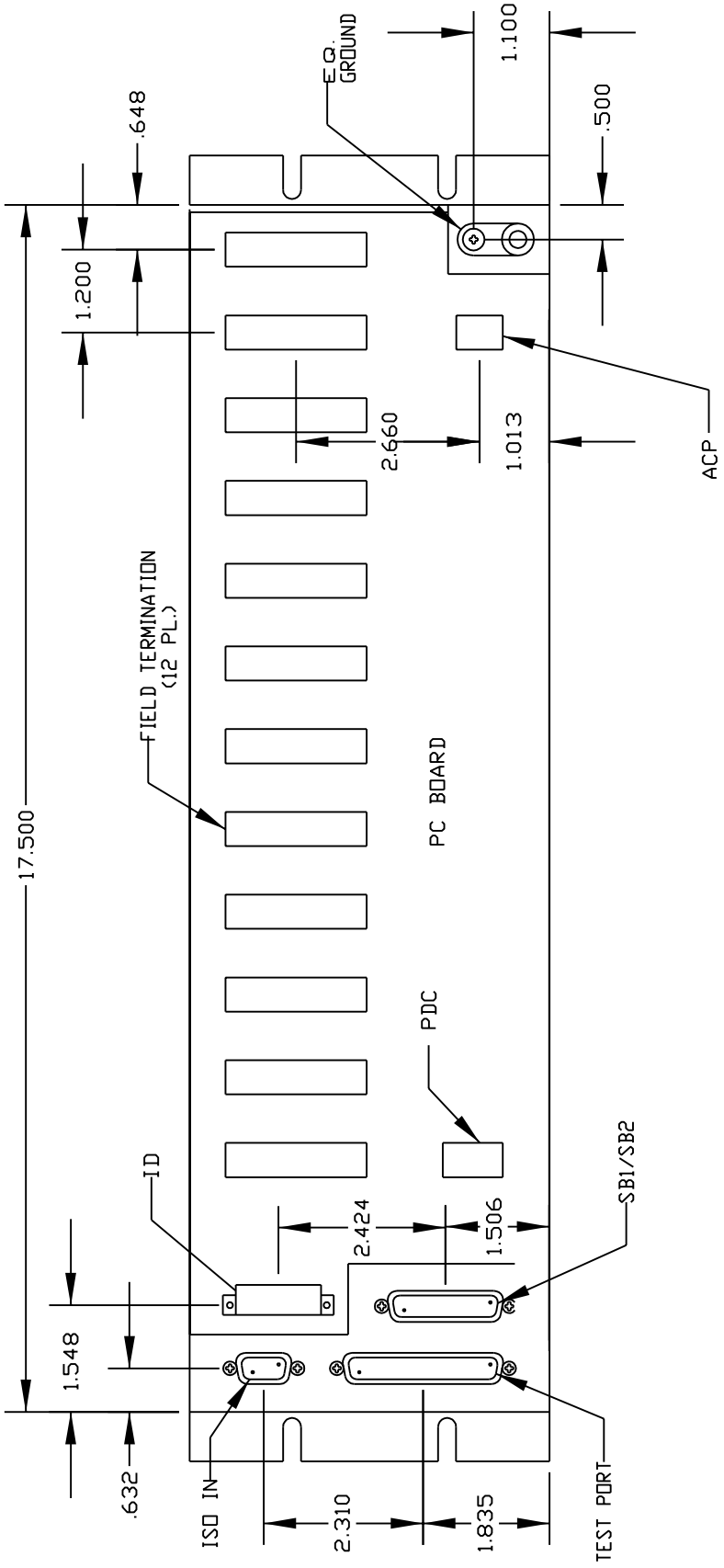
	NO SCALE	
	TEES, NOV 19, 1999	7-5-22



TITLE:

INPUT ASSEMBLY (FRONT VIEW)

	NO SCALE	
	TEES, NOV 19, 1999	7-5-23

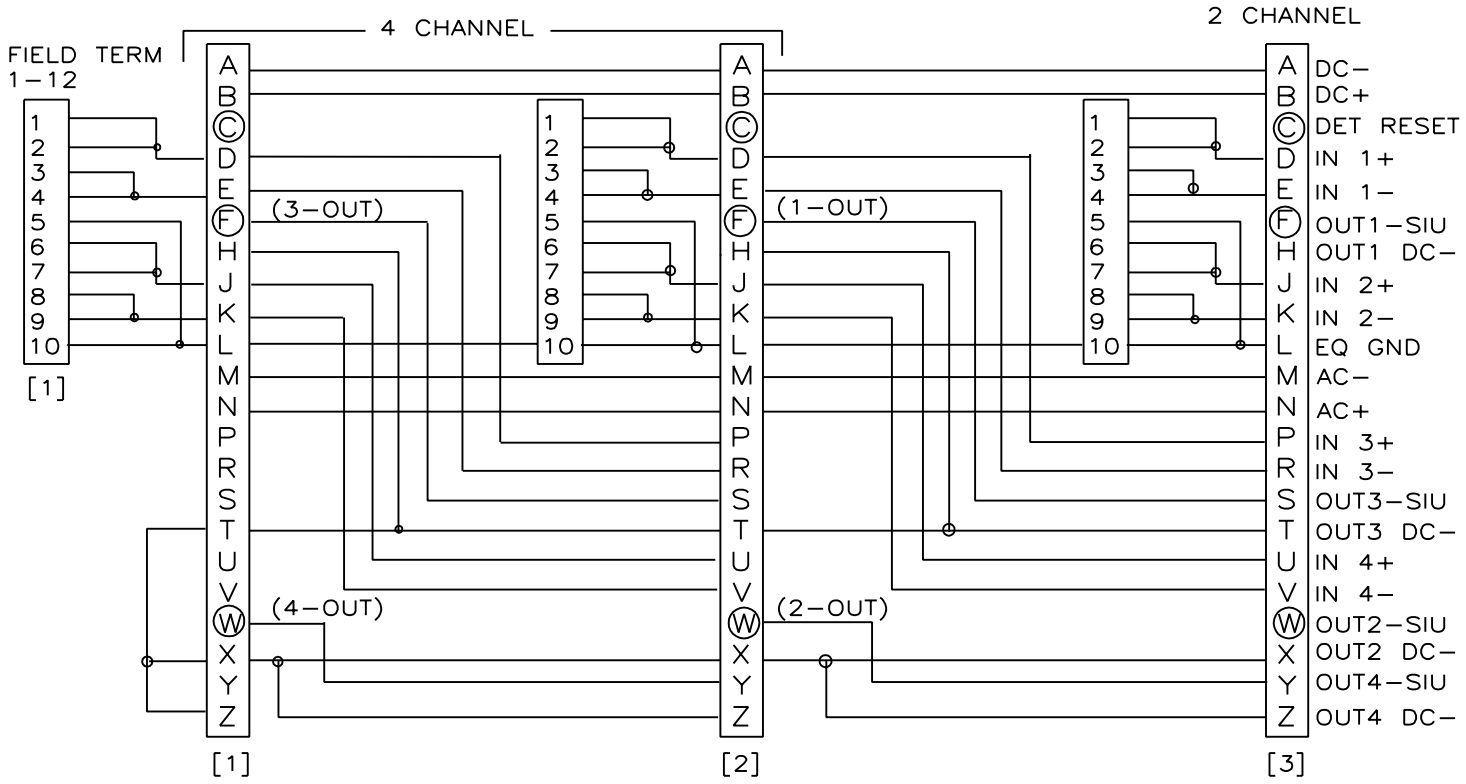


TITLE:

INPUT ASSEMBLY (REAR VIEW)

NO SCALE	
TEES, NOV 19, 1999	7-5-24

SLOTS 1–12 (12 2 CHANNEL DEVICES OR 6 4 CHANNEL DEVICES)

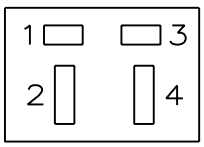


FIELD INPUT PANEL LETTERED SIDE

NUMBERED SIDE of Slots 1–12

1	NC
2	NC
3	Slot Address 3
4	IN 1+
5	IN 1–
6	Slot Address 0
7	1Status (slots 1–12)
8	IN 2+
9	IN 2–
10	Slot Address 1
11	AC–
12	AC+
13	IN 3+
14	IN 3–
15	Slot Address 2
16	3 Status (Slots 1–12)
17	IN 4+
18	IN 4–
19	TX Data
20	2 Status (Slots 1–12)
21	RX Data
22	4 Status (Slots 1–12)

PDC (Plug)



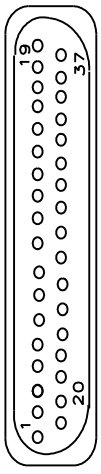
PDC (DC Power) CONNECTOR

Pin #	FUNCTION	SLOTS 1–12	Pin #	FUNCTION	SIU
PDC 3	+12VDC	B	PDC 1	+24VDC	1A,1B,1C
PDC 4	DC GROUND	A,T,H,X & Z	PDC 2	DC GROUND	32A,32B,32C

TEST CONNECTOR

Pin	SIU PIN	SIGNAL	Pin	SIGNAL	SIU PIN
1	B13	IN1	14	A20	IN14
2	A14	IN2	15	B20	IN15
3	B14	IN3	16	A21	IN16
4	A15	IN4	17	B21	IN17
5	B15	IN5	18	A22	IN18
6	A16	IN6	19	B22	IN19
7	B16	IN7	20	A23	IN20
8	A17	IN8	21	B23	IN21
9	B17	IN9	22	A24	IN22
10	A18	IN10	23	B24	IN23
11	B18	IN11	24	A25	IN24
12	A19	IN12	25	A32	DC Ground
13	B19	IN13	26 thru 37	NC	

TEST CONNECTOR (Plug)



ADDRESS CONNECTOR DETAIL

Pin #	FUNCTION	Pin #	FUNCTION
1	Address 1	2	DC GROUND
3	Address 2	4	DC GROUND
5	Address 4	6	DC GROUND
7	Address 8	8	DC GROUND

TITLE:

INPUT ASSEMBLY WIRING DIAGRAMS

NO SCALE

TEES, NOV 19, 1999

7–5–25

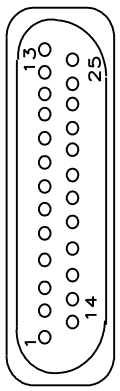
SIU CONNECTOR LIST

Pin #	FUNCTION	Pin #	DESTINATION & FUNCTION	Pin #	DESTINATION & FUNCTION
2A	Slot1C (Output1)	B23	Slot 11 F (Input21)	A1	PDC1 (+24VDC)
2B	Slot2C (Output2)	A24	Slot 11 W (Input22)	B1	PDC1 (+24VDC)
3A	Slot3C (Output3)	B24	Slot 12 F (Input23)	C1	PDC1 (+24VDC)
3B	Slot4C (Output4)	A25	Slot 12 W (Input24)	A32	PDC3 (24VDC Ground)
4A	Slot5C (Output5)	A10	S12-7 Stat1 (o17/i25)	B32	PDC3 (24VDC Ground)
4B	Slot6C (Output6)	B10	S12-20 Stat2 (o18/i26)	C32	PDC3 (24VDC Ground)
5A	Slot7C (Output7)	A11	S12-16 Stat3 (o19/i27)	B25	CDC1 (Opto Input 1)
5B	Slot8C (Output8)	B11	S12-22 Stat4 (o20/i28)	A26	CDC2 (Opto Input 2)
6A	Slot9C (Output9)	C3	Com 2 RXD+ (1TXD+)	B26	CDC3 (Opto Input 3)
6B	Slot10C(Output10)	C4	Com 15 RXD- (1TXD-)	A27	CDC4 (Opto Input 4)
7A	Slot11C(Output11)	C5	Com 1 TXD+ (1RXD+)	B27	CDC5 (Opto Input Common)
7B	Slot12C(Output12)	C6	Com 14 TXD- (1RXD-)	A28	ADC1 (Address-0)
B13	Slot 1 F (Input1)	C7	Com 4 RXC+ (1TXC+)	B28	ADC3 (Address-1)
A14	Slot 1 W (Input2)	C8	Com 17 RXC- (1TXC-)	A29	ADC5 (Address-2)
B14	Slot 2 F (Input3)	C9	Com 3 TXC+ (1RXC+)	B29	ADC7 (Address-3)
A15	Slot 2 W (Input4)	C10	Com 16 TXC- (1RXC-)	A30	Slot12-19 (INBUS TxD)
B15	Slot 3 F (Input5)	C11	Com 9 LSync+	B30	Slot12-21 (INBUS RxD)
A16	Slot 3 W (Input6)	C12	Com 22 LSync-	A/C31	EQ. GROUND
B16	Slot 4 F (Input7)	C13	Com 10 NReset+	B31	AC Line Reference
A17	Slot 4 W (Input8)	C14	Com 23 NReset-	C27	DC GROUND
B17	Slot 5 F (Input9)	C15	Com 11 PwrDwn+	C28	DC GROUND
A18	Slot 5 W (Input10)	C16	Com 24 PwrDwn-	C29	DC GROUND
B18	Slot 6 F (Input11)	C17	Com 6 RXD+ (2TXD+)	C30	DC GROUND
A19	Slot 6 W (Inpur12)	C18	Com 19 RXD- (2TXD-)		
B19	Slot 7 F (Input13)	C19	Com 5 TXD+ (2RXD+)		
A20	Slot 7 W (Input14)	C20	Com 18 TXD- (2RXD-)		
B20	Slot 8 F (Input15)	C21	Com 8 RXC+ (2TXC+)		
A21	Slot 8 W (Input16)	C22	Com 21 RXC- (2TXC-)		
B21	Slot 9 F (Input17)	C23	Com 7 TXC+ (2RXC+)		
A22	Slot 9 W (Input18)	C24	Com 20 TXC- (2RXC-)		
B22	Slot 10 F (Input19)	C25	INBUS TxC (TBD)		
A23	Slot 10 W (Input20)	C26	INBUS RxC (TBD)		

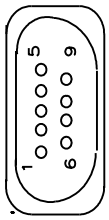
COM SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE SIU	Pin	AT THE CONTROLLER	AT THE SIU
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD-	SB1 RXD-
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD-	SB1 TXD-
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC-	SB1 RXC-
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC-	SB1 TXC-
5	SB2 TXD+	SB2 RXD +	18	SB2 TXD-	SB2 RXD-
6	SB2 RXD+	SB2 TXD +	19	SB2 RXD-	SB2 TXD-
7	SB2 TXC+	SB2 RXC+	20	SB2 TXC-	SB2 RXC-
8	SB2 RXC+	SB2 TXC+	21	SB2 RXC-	SB2 TXC-
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC-	LINE SYNC-
10	NRESET+	NRESET+	23	NRESET-	NRESET-
11	PWR DWN+	PWR DWN+	24	PWR DWN-	PWR DWN-
12	+5VDC ISO	+5VDC ISO	25	EQ GND	EQ GND
13	DC GND#2	DC GND#2			

COM SB1/SB2 (Socket)



CDC (PLUG)



CDC (Cabinet DC signal interconnect)

Pin #	FUNCTION	Pin #	FUNCTION
CDC-1	OPTO INPUT 1	CDC-2	OPTO INPUT 2
CDC-3	OPTO INPUT 3	CDC-4	OPTO INPUT 4
CDC-5	OPTO INPUT COMMON	CDC-6	Spare
CDC-7	Spare	CDC-8	Spare
CDC-9	Spare		

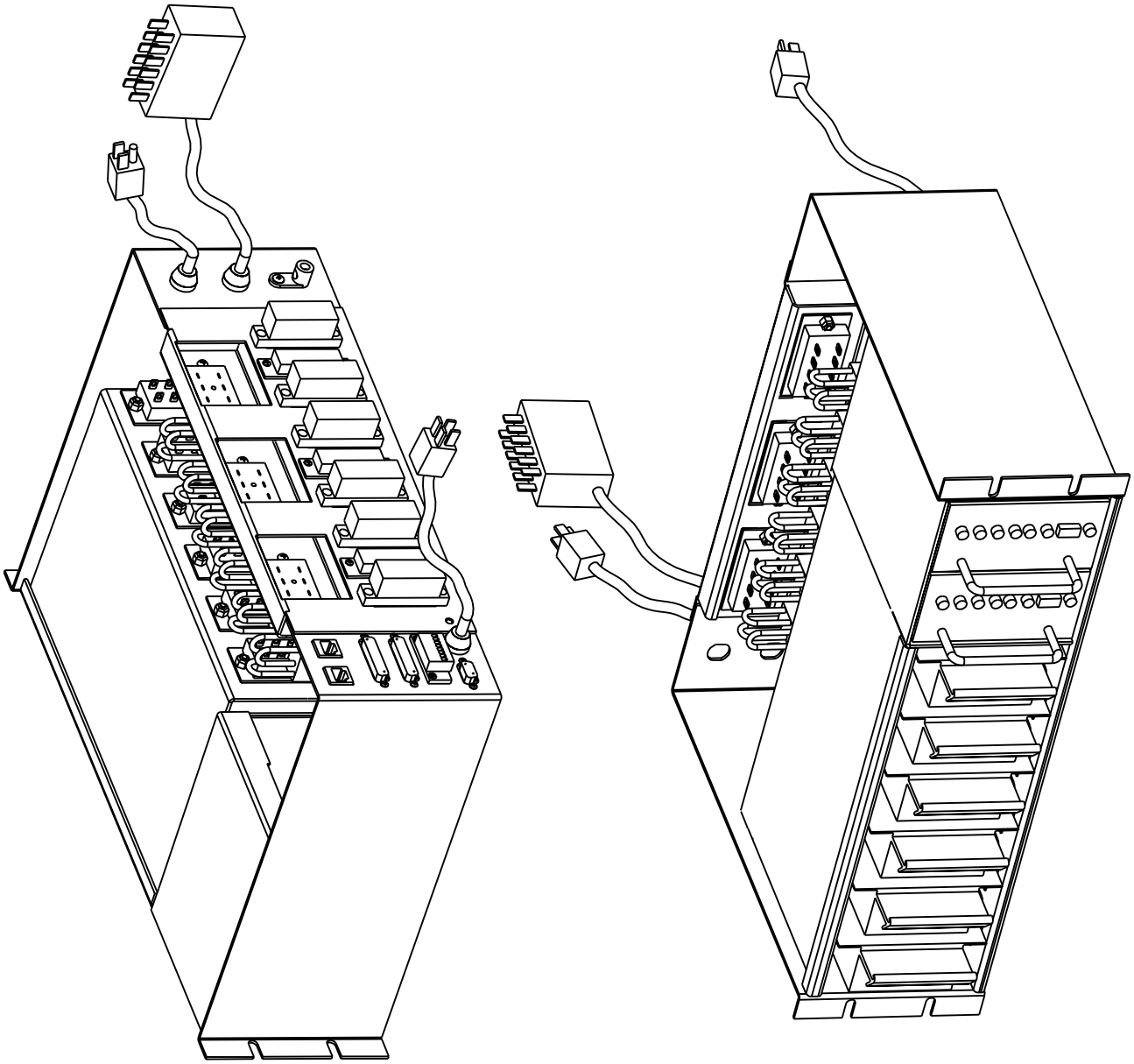
TITLE:

INPUT ASSEMBLY PIN ASSIGNMENTS

NO SCALE

TEES, NOV 19, 1999

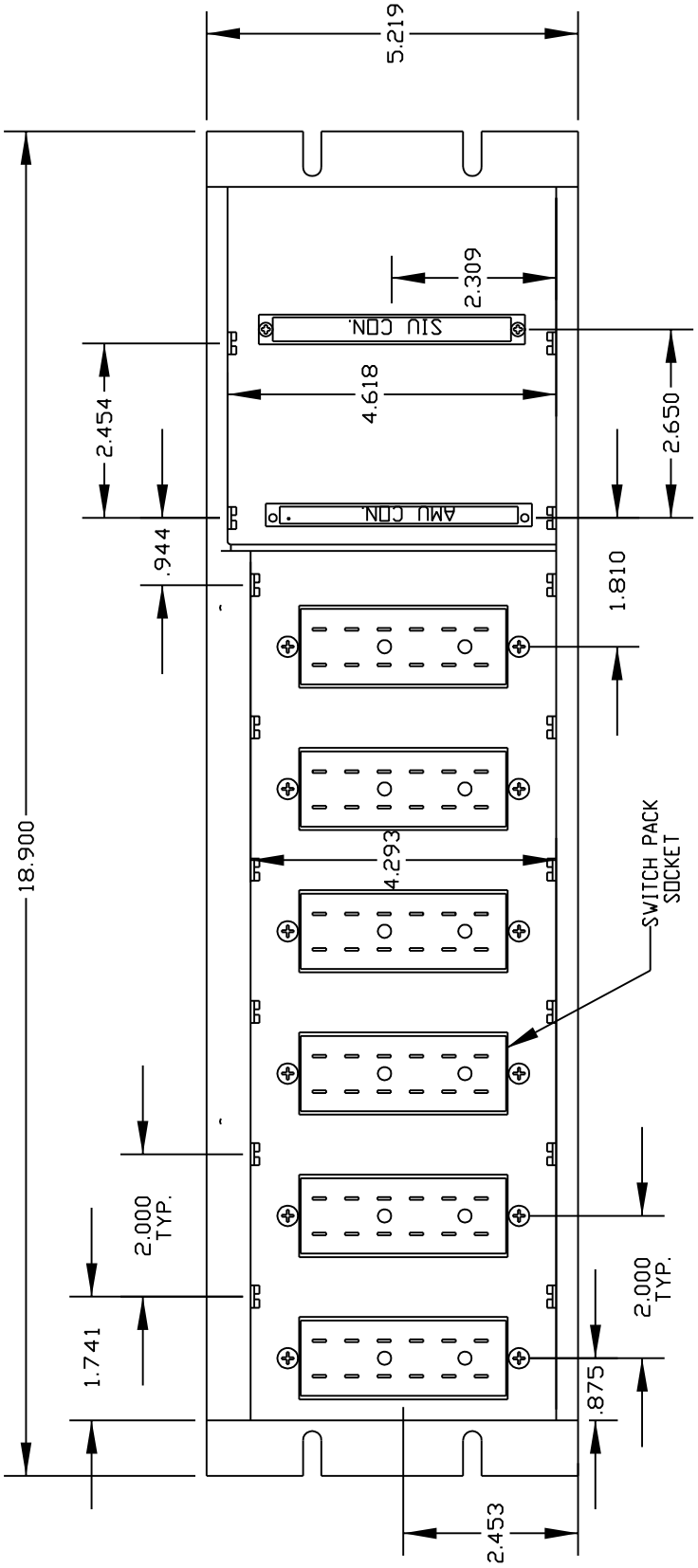
7-5-26



TITLE:

OUTPUT ASSEMBLY (DETAIL)

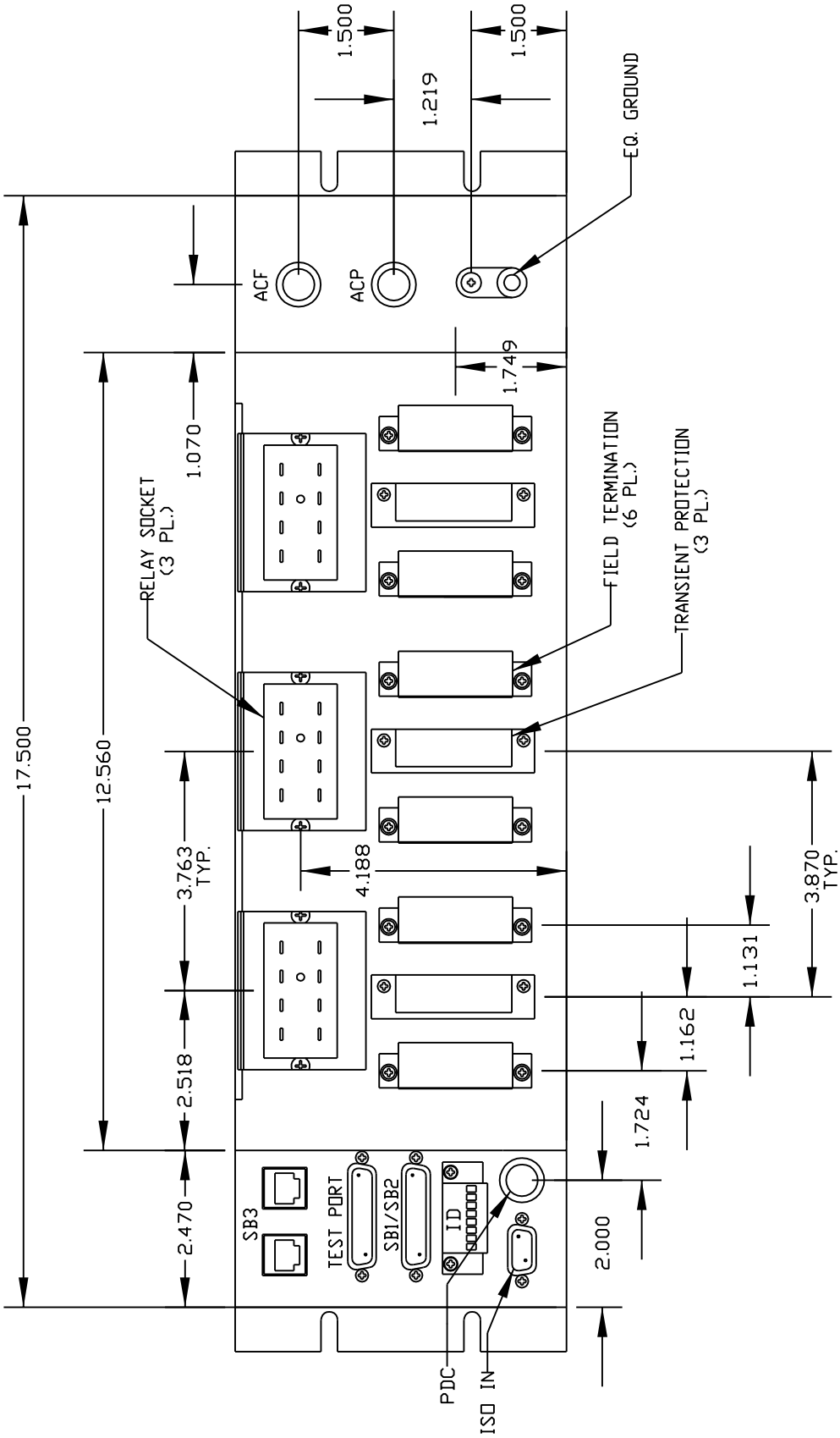
	NO SCALE	
	TEES, NOV 19, 1999	7-5-27



TITLE:

OUTPUT ASSEMBLY (FRONT VIEW)

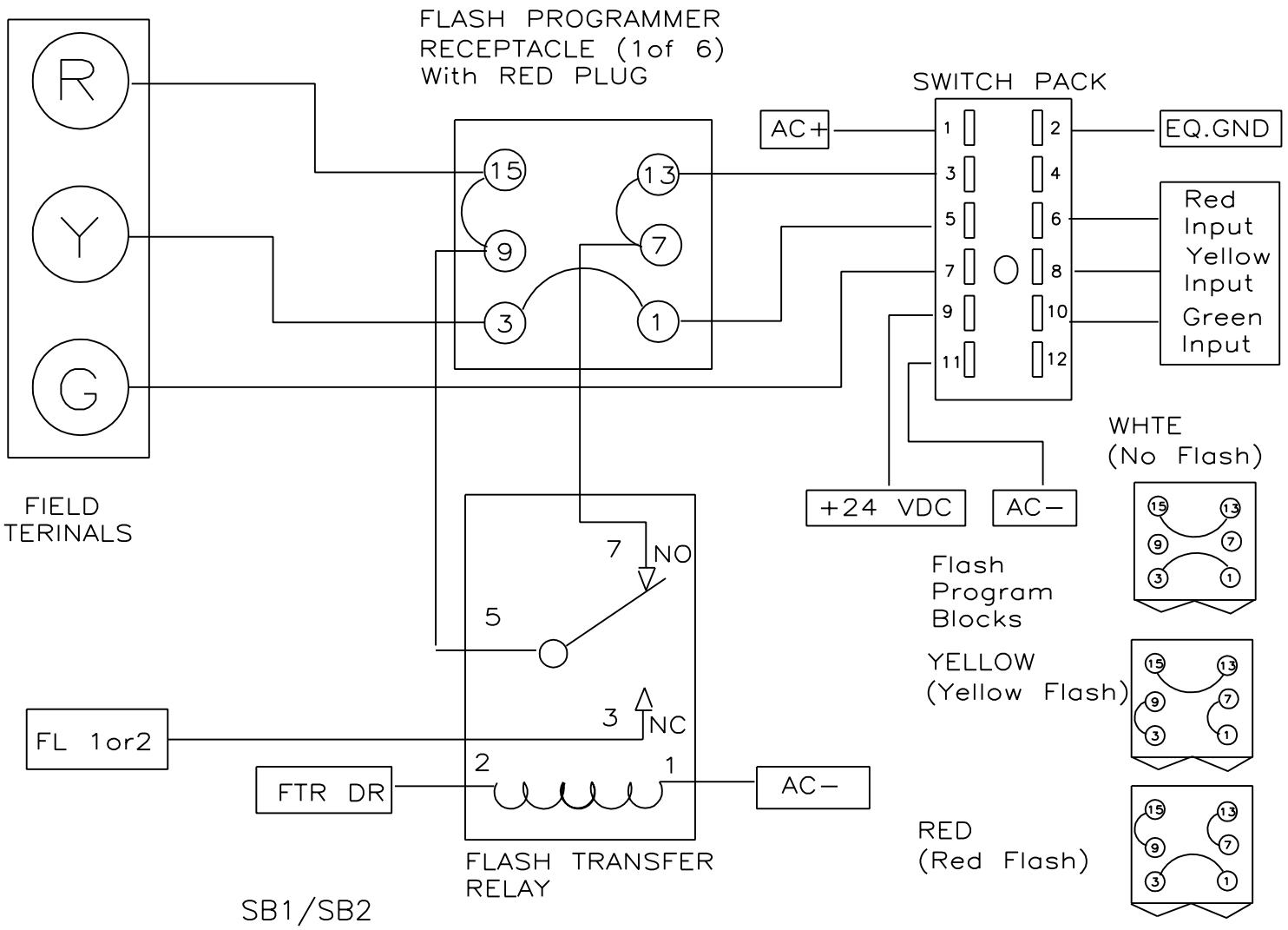
	NO SCALE	
	TEES, NOV 19, 1999	7-5-28



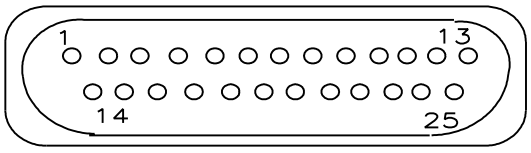
TITLE:

OUTPUT ASSEMBLY (REAR VIEW)

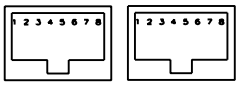
NO SCALE	
TEES, NOV 19, 1999	7-5-29



SB1/SB2
(Socket)



SB3 SOCKETS
WIRED IN
PARALLEL FOR
DAISY−CHAIN



SB3
(Sockets)

SB1/SB2 CONNECTOR

Pin	AT THE CONTROLLER	AT THE OUTPUT ASSY	Pin	AT THE CONTROLLER	AT THE OUTPUT ASSY
1	SB1 TXD+	SB1 RXD+	14	SB1 TXD−	SB1 RXD−
2	SB1 RXD+	SB1 TXD+	15	SB1 RXD−	SB1 TXD−
3	SB1 TXC+	SB1 RXC+	16	SB1 TXC−	SB1 RXC−
4	SB1 RXC+	SB1 TXC+	17	SB1 RXC−	SB1 TXC−
5	SB2 TXD+	NC	18	SB2 TXD−	NC
6	SB2 RXD+	NC	19	SB2 RXD−	NC
7	SB2 TXC+	NC	20	SB2 TXC−	NC
8	SB2 RXC+	NC	21	SB2 RXC−	NC
9	LINE SYNC+	LINE SYNC+	22	LINE SYNC−	LINE SYNC−
10	NRESET+	NRESET+	23	NRESET−	NRESET−
11	PWR DWN+	PWR DWN+	24	PWR DWN−	PWR DWN−
12	+5VDC ISO	+5VDC ISO	25	EQ GND	EQ GND
13	DC GND#2	DC GND#2			

SB3 CONNECTOR

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SP3 TXC+	SP3 RXC+
2	ORANGE	SP3 TXC−	SP3 RXC−
3	WHITE GREEN	DC GROUND	DC GROUND
4	BLUE	SP3 TXD+	SP3 RXD+
5	WHITE BLUE	SP3 TXD−	SP3 RXD−
6	GREEN	DC GROUND	DC GROUND
7	WHITE BROWN	SP3 RXD+	SP3 TXD+
8	BROWN	SP3 RXD−	SP3 TXD−

TITLE:

OUTPUT ASSEMBLY WIRING DIAGRAM

NO SCALE

TEES, NOV 19, 1999

7−5−30

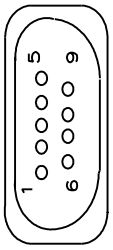
AMU CONNECTOR LIST

Pin #	TO FUNCTION	Pin #	TO FUNCTION	Pin #	TO FUNCTION
A18	LS1-3 (Output1)	A8	FTR1 COIL +	A31	FL1-1 (INPUT)
A19	LS1-5 (Output2)	B8	FTR1 COIL -	A32	FL1-2 (INPUT)
A20	LS1-7 (Output3)	A9	FTR2 COIL+	B31	FL2-1 (INPUT)
B18	LS2-3 (Output4)	B9	FTR2 COIL-	B32	FL2-2 (INPUT)
B19	LS2-5 (Output5)	A10	FTR3 COIL+	A1	PDC1 (+24VDC)
B20	LS2-7 (Output6)	B10	FTR3 COIL-	A2	PDC3 (24VDC Ground)
A21	LS3-3 (Output7)	A11	LS1 COIL+	B1	ADC1 (Address-0)
A22	LS3-5 (Output8)	B11	LS1 COIL-	B2	ADC3 (Address-1)
A23	LS3-7 (Output9)	A12	LS2 COIL+	B3	ADC5 (Address-2)
B21	LS4-3 (Output10)	B12	LS2 COIL-	B4	ADC7 (Address-3)
B22	LS4-5 (Output11)	A13	LS3 COIL+	A5	Com 7 RXD+ (3TXD+)
B23	LS4-7 (Output12)	B13	LS3 COIL-	B5	Com 8 RXD- (3TXD-)
A24	LS5-3 (Output13)	A14	LS4 COIL+	A6	Com 4 TXD+ (3RXD+)
A25	LS5-5 (Output14)	B14	LS4 COIL-	B6	Com 5 TXD- (3RXD-)
A26	LS5-7 (Output15)	A15	LS5 COIL+	A7	Com 1 TXC+ (1RXC+)
B24	LS6-3 (Output16)	B15	LS5 COIL-	B7	Com 2 TXC- (1RXC-)
B25	LS6-5 (Output17)	A16	LS6 COIL+	A2	Com 3 (Shield)
B26	LS6-7 (Output18)	B16	LS6 COIL-	A2	Com 5 (Shield)
A27	AC+ MAIN	B27	AC- MAIN	B29	EQ. GROUND

CDC LIST

Pin #	TO FUNCTION
CDC-1	B25 (MCE)
CDC-2	A26 (IA)
CDC-3	B26 (TIPS)
CDC-4	A27 (Spare)
CDC-5	B27 (0-In Common)
CDC-6	Spare
CDC-7	Spare
CDC-8	Ring (Test Plug)
CDC-9	24VDC Ground

CDC (Socket)



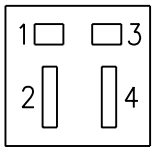
TEST CONNECTOR

Pin	SIU PIN	SIGNAL	Pin	SIGNAL	SIU PIN
1	A2	LS1 R	14	B8	LS5 Y
2	B2	LS1 Y	15	A9	LS5 G
3	A3	LS1 G	16	B9	LS6 R
4	B3	LS2 R	17	A10	LS6 Y
5	A4	LS2 Y	18	B10	LS6 G
6	B4	LS2 G	19	NA	
7	A5	LS3 R	20	NA	
8	B5	LS3 Y	21	NA	
9	A6	LS3 G	22	NA	
10	B6	LS4 R	23	NA	
11	A7	LS4 Y	24	NA	
12	B7	LS4 G	25	A32	DC Ground
13	A8	LS5 R			

SIU CONNECTOR LIST

Pin #	FUNCTION	Pin #	DESTINATION & FUNCTION	Pin #	DESTINATION & FUNCTION
A2	LS1-6 (Output1)	C3	Com 2 RXD+ (1TXD+)	A1	PDC1 (+24VDC)
B2	LS1-8 (Output2)	C4	Com 15 RXD- (1TXD-)	B1	PDC1 (+24VDC)
A3	LS1-10 (Output3)	C5	Com 1 TXD+ (1RXD+)	C1	PDC1 (+24VDC)
B3	LS2-6 (Output4)	C6	Com 14 TXD- (1RXD-)	A32	PDC3 (24VDC Ground)
A4	LS2-8 (Output5)	C7	Com 4 RXC+ (1TXC+)	B32	PDC3 (24VDC Ground)
B4	LS2-10 (Output6)	C8	Com 17 RXC- (1TXC-)	C32	PDC3 (24VDC Ground)
A5	LS3-6 (Output7)	C9	Com 3 TXC+ (1RXC+)	B25	CDC1 (Opto Input 1)
B5	LS3-8 (Output8)	C10	Com 16 TXC- (1RXC-)	A26	CDC2 (Opto Input 2)
A6	LS3-10 (Output9)	C11	Com 9 LSync+	B26	CDC3 (Opto Input 3)
B6	LS4-6 (Output10)	C12	Com 22 LSync-	A27	CDC4 (Opto Input 4)
A7	LS4-8 (Output11)	C13	Com 10 NReset+	B27	CDC5 (Opto Input Common)
B7	LS4-10 (Output12)	C14	Com 23 NReset-	A28	ADC1 (Address-0)
A8	LS5-6 (Output13)	C15	Com 11 PwrDwn+	B28	ADC3 (Address-1)
B8	LS5-8 (Output14)	C16	Com 24 PwrDwn-	A29	ADC5 (Address-2)
A9	LS5-10 (Output15)	C17	Com 6 RXD+ (2TXD+)	B29	ADC7 (Address-3)
B9	LS6-6 (Output16)	C18	Com 19 RXD- (2TXD-)	A30	Slot12-19 (INBUS TxD)
A10	LS6-8 (Output17)	C19	Com 5 TXD+ (2RXD+)	B30	Slot12-21 (INBUS RxD)
B10	LS6-10 (Output18)	C20	Com 18 TXD- (2RXD-)	A/C31	EQ. GROUND
B11	CDC8 (Ext Reset)	C21	Com 8 RXC+ (2TXC+)	C22	Com 21 RXC- (2TXC-)
B31	AC Line Reference	C23	Com 7 TXC+ (2RXC+)	C24	Com 20 TXC- (2RXC-)
C27	Option-0 Select ITS				

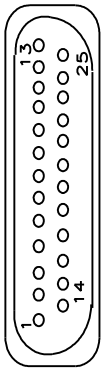
PDC (Plug)



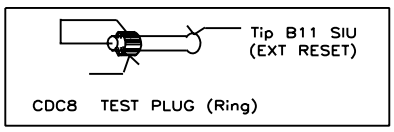
PDC LIST

Pin #	TO SIU
PDC-1	A,B,C1
PDC-2	A,B,C32
PIN #	TO AMU
PDC-1	A1
PDC-2	A2

TEST CONNECTOR (Plug)



TEST PLUG



ADDRESS CONNECTOR

Pin #	FUNCTION	Pin #	FUNCTION
1	Address 1	2	DC GROUND
3	Address 2	4	DC GROUND
5	Address 4	6	DC GROUND
7	Address 8	8	DC GROUND

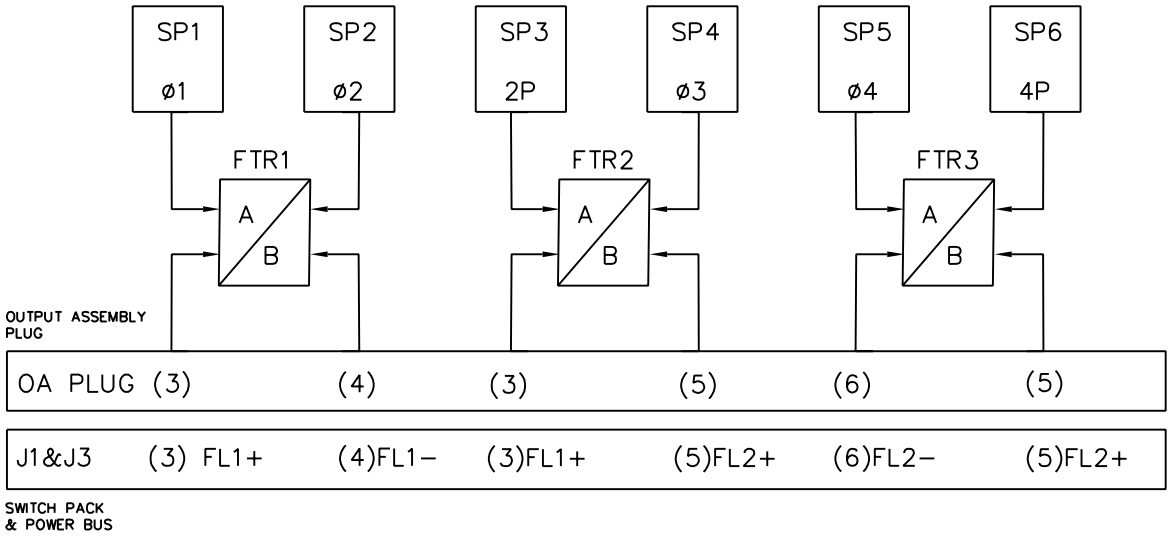
TITLE:

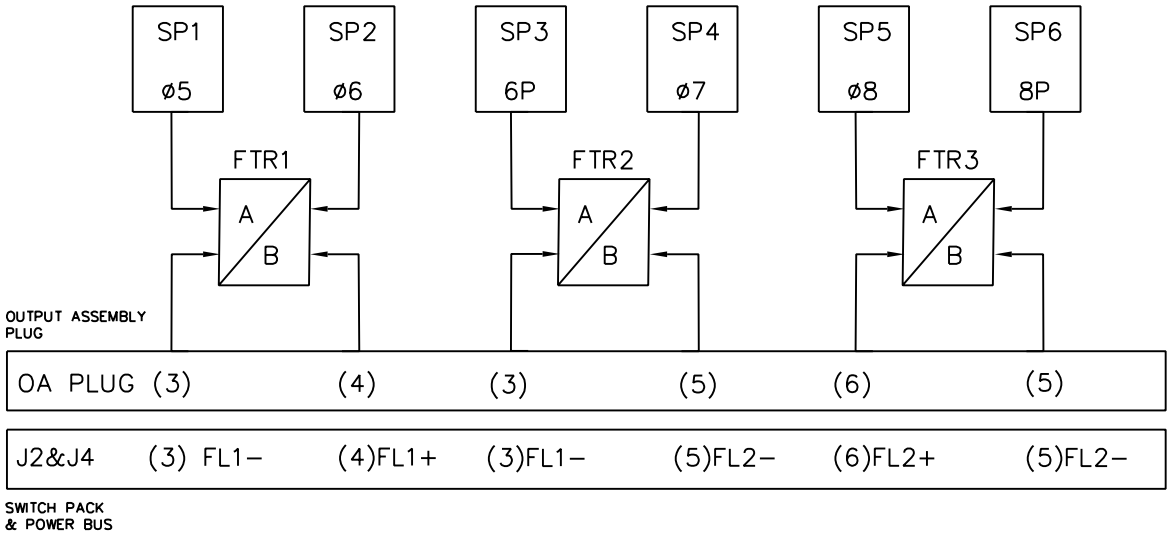
OUTPUT ASSEMBLY PIN ASSIGNMENTS

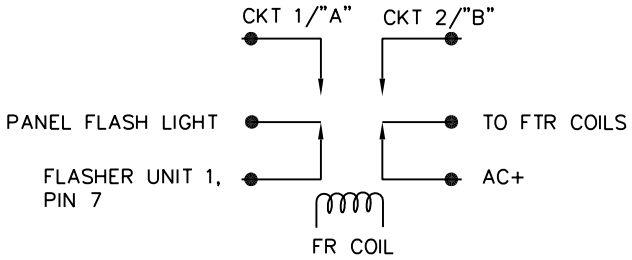
NO SCALE

NOV 19, 1999

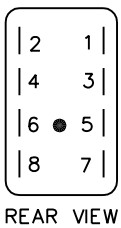
7-5-31







HEAVY DUTY (HD) RELAY SOCKET DETAIL



REAR VIEW

PIN	FUNCTION
1	COIL
2	COIL
3	N.C. CIRCUIT #1
4	N.C. CIRCUIT #2
5	COMMON CIRCUIT #1
6	COMMON CIRCUIT #2
7	N.O. CIRCUIT #1
8	N.O. CIRCUIT #2

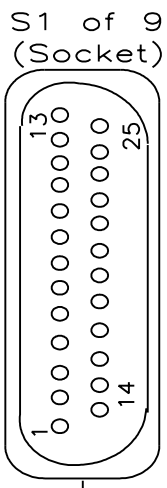
TITLE:

TRANSFER RELAY, FLASHER, LOADSWITCH WIRING

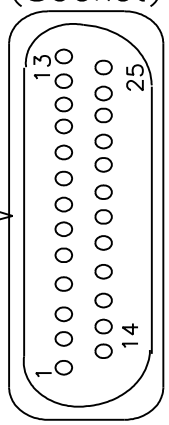
NO SCALE

TEES, NOV 19, 1999

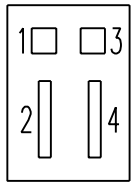
7−5−32



Pin	AT THE CONTROLLER	Pin	AT THE CONTROLLER
1	SB1 TXD+	14	SB1 TXD−
2	SB1 RXD+	15	SB1 RXD−
3	SB1 TXC+	16	SB1 TXC−
4	SB1 RXC+	17	SB1 RXC−
5	SB2 TXD+	18	SB2 TXD−
6	SB2 RXD+	19	SB2 RXD−
7	SB2 TXC+	20	SB2 TXC−
8	SB2 RXC+	21	SB2 RXC−
9	LINE SYNC+	22	LINE SYNC−
10	NRESET+	23	NRESET−
11	PWR DWN+	24	PWR DWN−
12	+5VDC ISO	25	EQ GND
13	DC GND#2		

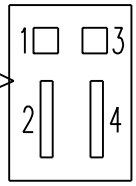


HARNESS (COMMUNICATIONS BUS)



PDC (DC Power) CONNECTOR

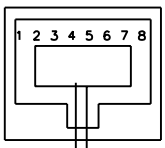
Pin #	FUNCTION	Pin #	FUNCTION
PDC 1	+24VDC	PDC 3	+12VDC
PDC 2	DC GROUND	PDC 4	DC GROUND

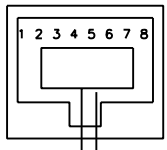


HARNESS (DC Power BUS)

HARNESS (SB3)

Pin #	PAIR COLOR	AT THE PDA	AT THE OUTPUT ASSEMBLY
1	WHITE ORANGE	SP3 TXC+	SP3 RXC+
2	ORANGE	SP3 TXC−	SP3 RXC−
3	WHITE GREEN	DC GROUND	DC GROUND
4	BLUE	SP3 TXD+	SP3 RXD+
5	WHITE BLUE	SP3 TXD−	SP3 RXD−
6	GREEN	DC GROUND	DC GROUND
7	WHITE BROWN	SP3 RXD+	SP3 TXD+
8	BROWN	SP3 RXD−	SP3 TXD−





TITLE:
CONTROL / SERIAL BUS & SERIAL BUS#3 HARNESSES

NO SCALE	
TEES NOV 19, 1999	7−5−33

CHAPTER 9

SPECIFICATION FOR MODEL 2070

CONTROLLER UNIT

(2070 UNIT)

TABLE OF CONTENTS

CHAPTER 9 SECTION 1

GENERAL

9.1.1
The Controller Unit shall be composed of the UNIT CHASSIS, modules and assemblies. The following is a list of composition deliverables associated to items:

UNIT VERSION	DESCRIPTIVE
2070 UNIT	Full unit mated to 170 cabinet family
2070N UNIT	Full unit mated to TS1 cabinet family
2070L UNIT	LITE Unit mated to 170 cabinet family
2070LC UNIT	LITE unit mated to ITS & TS2 cabinet families
2070LCN UNIT	LITE unit mated to TS1 cabinet Family

ITEM DESCRIPTION		UNIT VERSIONS 2070	2070N	2070L	2070LC	20070LCN
UNIT CHASSIS		1	1	1	1	1
Model 2070-1A	Two Board CPU	1	1	-	-	-
Model 2070-1B	One Board CPU	-	-	1	1	1
Model 2070-2A	Field I/O for 170 Cab	1	1	1	-	-
Model 2070-2B	Field I/O for ITS /NEMA Cab	-	1	-	1	1
Model 2070-3A	Front Panel-Display A	1	1	-	-	-
Model 2070-3B	Front Panel-Display B	-	-	1	-	-
Model 2070-3C	Front Panel-Blank	-	-	-	1	1
Model 2070-4A	Power Supply- 10 AMP	1	1	-	-	-
Model 2070-4B	Power Supply- 3.5 AMP	-	-	1	1	1
Model 2070-5A	VME Cage Assembly	1	1	-	-	-
Model 2070-5B	MCB 1A Mounting Assembly-					
Model 2070-8	NEMA Interface Module	-	1			1
Model 2070-9	2070N Back Cover	-	1			1

9.1.2
The communications and option modules/assemblies shall be called out separately from the unit version. The composition weight shall not exceed 11.3 kilograms.

9.1.3
The CHASSIS Enclosure, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Cover Plates, Power Supply Enclosure, and Front Panel shall be made of 1.524 mm minimum aluminum sheet.

9.1.4
2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A&B FPA	500 mA	-----	50 mA	50 mA

2070-3C FPA	**100 mA**	**-----**	**50 mA**	**50 mA**
2070-5 VME Cage	**5.0 A**	**-----**	**200 mA**	**200 mA**
2070-6 All Comm	**500 mA**	**-----**	**100 mA**	**100 mA**
2070-7 All Comm	**250 mA**	**-----**	**50 mA**	**50 mA**

9.1.5
All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.

9.1.6
The EIA-485 Line Drivers/Receivers shall be socket mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.7
A Mean-Time-Between-Failure Analysis Report shall be provided with the Qualified Products List Submittal. It shall encompass the 2070 Unit (complete) and its individual modules / assemblies. The report shall describe in detail the methodology used.

9.1.8
Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.9
SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	**SP3**
CPU 2070-1	**“ 19"**	**“19”**
FI/O 2070-2A & -8	**" 20"**	**“NA”**
CPU Broadcast to all	**"127"**	**“255”**

All other addresses are reserved by the AGENCY. The SDLC response frame address shall be the same address as the Command frame it receives.

9.1.10
The 2070 UNIT shall comply with the AGENCY Year 2000 Compliance:
"Year 2000 compliance for Systems in the AGENCY is achieved when an application or system products (including software, microcode and microprocessors), programs, files, databases, and functionality have or create no logical or mathematical inconsistencies when dealing with dates prior to and beyond 1999. The year 2000 is recognized and processed as a leap year. The product must also operate accurately in the manner in which it was intended for date operation without requiring manual intervention."

CHAPTER 9 SECTION 2

MODEL 2070-1 CPU MODULE

9.2.1
The MODEL 2070-1A CPU shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

9.2.2
The MODEL 2070-1B CPU shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the MOTHERBOARD Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7 except for the following:

9.2.2.1
The VME software and hardware bus requirements shall not apply nor do the MCB and Board Interface Harness physical requirements.

9.2.2.2
A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements including EIA 485 drivers / receivers and synchronous bps rate of 614 Kbps. A internal LOGIC Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6,7,18,19 and 20) lines from C13S Connector.

9.2.2.3
The 68360 SCC1 shall be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802-3 (TP) 10 BASE T Standard Requirements, both hardware and software. The four network lines shall be used to route ETHERNET across the MOTHERBOARD to the "A" Connectors. DC Grounding plane around the network connectors and lines shall be provided. Network Lines shall be assigned as: Network 1 = ENET TX+, Network 2 = ENET TX-, Network 3= ENET RX+, and Network 4 = ENET RX-. In addition, the conditioned ETHERNET shall be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel. Four LEDs labeled "TX, RX, TX Collision, and TX Status" shall be mounted on the front panel signifying ETHERNET operational conditions.

9.2.2.4
The 2070-1B CPU shall not draw more than 1.25 A of +5VDC & 500 mA of ISO+12 VDC.

9.2.3
MAIN CONTROLLER BOARD (MCB)

9.2.3.1
The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO (64).

9.2.3.2
The CONTROLLER Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for State use only. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7, ACFAIL
Level 6 - VMEbus IRQ6
Level 5 - VMEbus IRQ5, CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4- VMEbus IRQ4
Level 3 - VMEbus IRQ3
Level 2 - VMEbus IRQ2
Level 1 - VMEbus IRQ1

9.2.3.3
MEMORY ADDRESS ORGANIZATION

8000 0000 - 80FF FFFF	**STANDARD**
9000 0000 - 9000 FFFF	**SHORT**

9.2.3.3.1
16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's RBF Manager. The address of each memory block shall be specified by the Contractor and provided with the documentation.

9.2.3.3.2
When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. A on-board circuit shall sense the +5 VDC Standby Power and shift to a On-board CPU Power source. The CPU On-board Power shall be capable of holding the SRAM and TOD Clock up for 30 Days. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.3.4
RAM MEMORY - A minimum of 4 MB of DRAM, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM, organized in 16- or 32-bit words, shall be provided. The SRAM shall draw no more than 50 μA at +5 VDC in Standby Mode. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.3.5
FLASH MEMORY - A minimum of 4 MB of FLASH Memory, organized in 16- or 32-bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control. No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for AGENCY use.

9.2.3.6
TIME-OF-DAY CLOCK - A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall, under on-board standby power, operate for a minimum of 30 days

maintaining an accuracy of ±1 minute per 30 days at 25° C. The clock shall be alined to a minimum fractional second resolution of 10 ms and shall track seconds, minutes, hours, day of month, month, and year.

9.2.3.7
A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be driver capable of sinking 30 mA at 30 VDC. Execution of the program module "CPURESET" in the boot image shall assert the CPU RESET signal once.

9.2.3.8
An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED INDICATOR.

9.2.3.9*
The OS-9 Operating System TICK Timer shall be derived from the each transition of LINESYNC with a tick rate of 120 ticks per second.

9.2.4*
A TRANSITION Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard. Said signal and communication lines shall be driven/received off and on the module compliant to EIA- 485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 &A3 INSTALLED lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

9.2.5
A SHIELDED INTERFACE HARNESS shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.

9.2.6
DATA KEY - A DATAKEY Receptacle (KC4210, KC4210PCB or equal) with Key (DK1000or equal) resident shall be provided and mounted on the CPU module front panel (or the Transition Board of Model 1A). The Black DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface. Power shall not be applied to the receptacle if the key is not present.

9.2.7
CPU MODULE SOFTWARE - The following shall be supplied:

1. **Operating System**
2. **Drivers and Descriptors**
3. **Application Kernel**
4. **Error Handler**
5. **Validation Suite**
6. **Deliverables**

9.2.7.1
OPERATING SYSTEM - The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.03 or later software and, in addition, the following:

1. **Embedded OS-9 Real Time Kernel**
2. **Sequential Character File Manager (SCFMAN)**

3. **Sequential Protocol File Manager (SPFMAN)**
4. **Pipe File Manager (PIPEMAN)**
5. **Random Block File Manager (RBFMAN)**
6. **C Input Output Library (CIO)**

Boot Image shall include the following utility modules:

Break	**Date**	**Deiniz**	**Devs**	**Free**	**Copy**
Dir	**Tmode**	**Edt**	**List**	**Load**	**Deldir**
Dump	**Del**	**Ident**	**Iniz**	**Irqs**	**Events**
Echo	**Kill**	**Dcheck**	**Cio**	**Link**	**Kermit**
Lmm	**Mdir**	**Mfree**	**Pd**	**Makdir**	**Save**
Attr	**Rename**	**Procs**	**Unlink**	**Sleep**	**Xmode**
Shell	**Build**	**Setime**			

9.2.7.2
DRIVERS AND DESCRIPTORS

9.2.7.2.1
Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

9.2.7.2.2
Drivers shall be provided to access the FLASH, SRAM, and DRAM memories through RBFMAN. The following RBFMAN descriptors shall apply:

/d0	**Floppy Diskette Drive**	**Reserved name; no driver required**
/f0	**FLASH Drive**	**Accessed as RAM disk & OS-9 /dd default Device**
/h0	**Hard Disk Drive**	**Reserved name; no drive required**
/r0	**SRAM Drive**	**Accessed as RAM disk**
/r1		**Reserved; no driver required**
/r2	**Temporary DRAM Drive**	**Allows 1 MB of DRAM, accessed as RAM disk; not initialized at boot time**

9.2.7.2.3
A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be through SCFMAN using the following descriptors:

9.2.7.2.3.1
Descriptor names for each timer:

timer 1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 [cascaded]
timer34 = access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.2.3.2
Timer descriptor option structure: The driver shall change appropriate timer functions only and ignore values that do not apply to a particular timer function. The data structure is as follows:

```
typedef struct {
    // Timer Global Configuration Register Related Options:
```

```
        rserveTGCR  :11;                                                    (MSB)
        timerCAS    :1;     // Cascade timers
        timerFRZ    :1;     // Freeze
        timerSTP    :1;     // Stop timer
        timerRST    :1;     // Reset timer
        timerGM     :1;     // Gate mode                    default = 0    (LSB)

        // Timer Mode Register Related Options:
        timerPS     :8;     // Prescale value               default = 0    (MSB)
        timerCE     :2;     // Capture vdge & enable interrupts  default = 0
        timerOM     :1;     // Output mode                  default = 0
        timerORI    :1;     // Output reference interrupt enable  default = 0
        timerFRR    :1;     // Free Run or Restart          default = 0
        timerICLK   :2;     // Input Clock Source           default = 1
        timerGE     :1;     // Gate Enable;                 default = 0    (LSB)

        // Timer Reference Register
        U_INT16     timerTRR                                default = 0

        // Timer Capture Register
        U_INT16     timerTCR                                default = 0xffff

        // Timer Event Register
        reserveTER  :14;    // Reserve                                     (MSB)
        timerREF    :1;     // Output reference event       default = 1
        timerCAP    :1;     // Capture event                default = 1    (LSB)
    } TTimer_opts;
```

9.2.7.2.3.3

Standard OS-9 SCFMAN Function Calls:

```
error_code  _os_open (char *timer_desc_name, path_id *path);
error_code  _os_close (path_id path);
error_code  _os_gs_popt (path_id path, u_int32*sizeof(TTimer_opts), void *timer_opts);
error_code  _os_ss_popt (path_id path, u_int32*sizeof(TTimer_opts), void *timer_opts);
error_code  _os_write (path_id path, void *timer_value, 4);
error_code  _os_read (path_id path, void *timer_value, 4);
```

9.2.7.2.4

The OS-9 SCFMAN shall provide access to the CPU Datakeyand its control through the following descriptor name and OS-9 functions:

Descriptor name:

datakey =CPU Datakey

Function Calls:

```
error_code_os_open(char*datakey_desc_name, path_id*path);
        error_code= E$NotRdy if CPU Datakey is not installed
error_code_os_read(path_id_path, void*control,128);
        error_code=E$NotRdy if CPU Datakey is not inserted
error_code_os_close((path_id path);
```

9.2.7.2.5

The async-communications serial device driver shall operate in six modes described below to accommodate communications network (EIA 232) and their associated flow control mode number (FCM #).

FCM# Description

0) No Flow Control Mode: The CTS and CD signals are set asserted internally, so the serial device driver can receive data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. This is the default mode for Model 2070 controllers. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode.

1) Manual Flow Control Mode: The serial device driver transmits and receives data regardless of the RTS, CTS, and CD states. The user program has absolute control of the RTS state and can inquire of the states of CTS and CD. The states of CTS and CD are set externally by a DCE. The device driver doesn't assert or de-assert the RTS.

2) Auto-CTS Flow Control Mode: The serial device driver transmits data when CTS is asserted. The CTS state is controlled externally by a DCE. The user program has absolute control of the RTS state. The CD is set asserted internally. The device driver doesn't assert or de-assert the RTS.

3) Auto-RTS Flow Control Mode: The CTS and CD are set asserted internally. The serial device driver receives and transmits data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. If the user program asserts the RTS, the RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty. Parameters related to delays of the RTS turn-off after last character are user configurable.

4) Fully Automatic Flow Control Mode: The serial device driver receives data when CD is asserted. Upon a write command, the serial device driver asserts RTS and wait for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed. Parameters related to delays of RTS turn-off after last character are user configurable. If user program asserts the RTS, RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty.

5) Dynamic Flow Control Mode: The Serial device driver maintains a transmit buffer and a receive buffer with fixed sizes, controls the state of RTS and monitors the state of CTS. The transmission and reception of data are managed automatically by the serial device driver. The serial device driver transmits data when CTS is asserted. The serial device driver asserts RTS when its receiving buffer is filled below certain level (low watermark), and de-asserts RTS when its receiving buffer is filled above certain level (high watermark).

The serial device driver shall be able to accept user configuration commands to configure the device driver via OS9_os_ss_size() function call and to accept user request commands for status of serial port from the device driver via OS9_os_gs_size() function call.

The single 32-bit variable passed by_os_ss_size() is defined as follow:

a) Flow Control Code is SS_OFC (0x23):

Bits Description
31-24 Auto RTS turn-off extension count in number of characters (range=0-255 1=default).
15 Auto RTS turn-off extension timing (0=bps rate=default, 1=equivalent 1200 bps).
14-13 Reserve for Future Use (default=0).
12 Inhibit Change of SCC MRBLR for opened path (default =0; 0=NO; 1=inhibit).
11 Inhibit SCC TODR for opened path (default=0; 0=NO; 1=inhibit).
10-8 Flow Control Mode Number (FCM#) (range=0-5).
7-0 Flow Control Code (FCC) =0x23

Note: The RTS turn-off extension can represent a bps rate independent time value rather a number of character times, (higher bps rates are normalized to equivalent 1200 bps characters) when selected by bit 15=1. Thus, a value of 4 represents the time of four characters at 1200 bps even when the actual rate is 9600. If bit 15=0, then an extension value = 4 represents 4 characters, which at a bps rate of 9600 would extend the RTS by approximately 3.3 ms.

b) Flow Control Code is SS_IFC (0x22):

Bits Description
31-22 Flow Control Mode 5 high water mark value (range=1-1023; default=256).
21-12 Flow Control Mode 5 low water mark value (range=1-1023; default=256).
11 Inhibit DCD activating control (default=0; 0=off; 1=on).
10 DCD flow control is active (default=0; 0=NO; 1=YES, changed by FCM#).
9-8 Reserved for Future Use (default=0).
7-0 Flow Control Code (FCC) = 0X22.
Note: The inhibit DCD selection has priority over the DCD ON request in the same access. Therefore, sending 0x0000022 results in DCD inhibit and DCD Flow Control inactive for all Flow Modes. A new flow control mode number shall set DCD function to that required in the new mode unless DCD is inhibit is ON.

c) Flow Control Code is SS-Ssig (0x1a):

Bits Description
31-16 A signal number to be sent to calling process when the state of a pin is changed.
15-14 Reserved for Future Use (default=0).
13 Ring is asserted (capable hardware only).
12 CTS is de-asserted.
11 CTS is asserted.
10-8 Reserved for Future Use (default=0).
7-0 Flow Control Code (FCC) = 0x1a.

d) Flow Control Code is SS-DCmd (0x0d):

Bits Description
31-15 Reserved for Future Use (default=0).
14 De-assert DTR (capable hardware only).
13 Assert DTR (capable hardware only).
12 De-assert RTS (duplicated function with_os_ss_DsRTS();).
11 Assert RTS (duplicated function with_os_ss_EnRTS();).
10-8 Reserved for Future Use (default=0).
7-0 Flow Control Code (FCC)=0x0d.

The single 32-bit variable returned by_os_gs_size() is defined as follow:

Bits	Description
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use (default=0).
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Used (default=0).
6	Overrun error –0=no error; 1=error on last received character.
5	Frame error –0=no error; 1=error on last received character.
4	Parity error –0=no error; 1=error on last received character.
3	Ring state –0=de-asserted; 1=asserted (capable hardware only).
2	DSR state –0=de-asserted; 1=asserted (capable hardware only).
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

9.2.7.2.6
Four input buffering modes shall be provided:

1.Line - characters are buffered up to and including a programmable termination character.

2.Fixed -a fixed specific number of characters is buffered by the driver.

3.Timed- characters are buffered until a programmable inter-character time out occurs.

4. Raw – characters are unbuffered and delivered to the task as received.

9.2.7.2.7
Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.

9.2.7.2.8
Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator
dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code  _os_open (char *desc_name, path_id *path);     //open descriptor for command
error_code  _os_close (path_id path);                      //close descriptor
error_code  _os_write (path_id path, void *value, 1);      //set value or function
        *value = 1, turn led on or turn DLSclock feature on (default)
        *value = 0, turn led off or turn DLSclock feature off
error_code  _os_read (path_id path, void *value, 1);       //get current state
```

9.2.7.2.9
TIME OF DAY (TOD) CLOCK - The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.2.9.1
Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.

9.2.7.2.9.2
Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.2.9.3
Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

9.2.7.2.10
The FLASH RAM drive (/f0) shall be protected from corruption due to power failure during a write operation. The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose. A large file being written, but truncated due to power fail, shall not be restored intact.

9.2.7.3
APPLICATION KERNEL

9.2.7.3.1
The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 & 2	**1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo**
SP 3S	**614.4 Kbps**
SP4	**9.6 Kbps, 8-bit word, 1 stop, no parity, no pause,XDR off,xoff**
SP 5S	**614.4 Kbps**
SP 6	**38.4 Kbps, 8-bit word, 1 stop and no parity**

9.2.7.3.2
Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

9.2.7.3.3
A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

9.2.7.3.4
After initialization (boot up from SYSRESET), the program shall fork to the defined module in FLASH memory named OPEXEC preceded by a full path. If OPEXEC is not found or fails the program shall fork a shell. If OPEXEC is forked successfully, the program shall exit.

9.2.7.3.5
A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. A Short Out results in resumption of Application Software without an operating system reboot. The Contractor shall provide a documented method for the Application Software to recover from Level 7 IRQ (ACFAIL) without a SYSRESET. A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.4
ERROR HANDLER

9.2.7.4.1
Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

9.2.7.4.2
The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

1. **Timer initialization error**
2. **Timer power up test error**
3. **Serial communication port initialization error**
4. **Serial communication port power up test error**
5. **Peripheral component initialization error**

9.2.7.4.3
The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

9.2.7.5
VALIDATION SUITE

9.2.7.5.1
A validation suite of software and associated documentation shall be provided. It shall include all diagnostic programs necessary to test all 2070 UNIT functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program all functions

9.2.7.5.2
Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

9.2.7.5.3
When factory boot code is operating without the User "Opexec" started, the Validation Suite shall be invoked from the front panel keypad, either as a execution in a continuous loop or by individual test selections.

9.2.7.5.4
The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. If the User Program has been executed, the VALSUITE shall not execute any of its tests due to resource conflicts. It shall be possible to execute the following additional CPU Module specific commands while in the OS-9 Shell Utility:

1. **Get/Set the hardware time of day clock**
2. **Set OS-9 clock from hardware clock**
3. **Read/write all I/O registers internal to the MC 68360**
4. **Get/Set all programmable controls on serial ports**
5. **Verify that the 120 Hz interrupt is functioning**
6. **Set, configure, and read timers**
7. **Observe time-out interrupts**

9.2.7.5.5
The OS-9 Shell Utility shall communicate with the user through the SP4 Port. When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form *"port P hh:mm:ss."* P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.

9.2.7.5.6*
Source and object Software shall be provided to the QPL or Purchasing Agency on both document listing and CD Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non- exclusive rights to this program suite.

9.2.7.6
DELIVERABLES

9.2.7.6.1
A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.

9.2.7.6.2
All software shall be delivered in the following forms:

1. **Fully commented source code of contractor developed software (OS-9 not required)**
2. **Microware Ultra-C Version 1.1 compatible linkable object code**
3. **Memory map listing**

9.2.7.6.3
Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.

9.2.7.6.4
Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

9.2.7.6.5
Software to initialize and perform a power-up self-test of the CPU Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.

9.2.7.6.6
OS-9 compliant header files shall be provided with all Driver Modules.

CHAPTER 9 SECTION 3

MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1
The MODEL 2070-2A MODULE shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2
The MODEL 2070-2B MODULE shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3
FIELD CONTROLLER UNIT (FCU) - The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware.

9.3.4
PARALLEL I/O PORTS - The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

9.3.4.1
The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2
Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5
OTHER MODULE CIRCUIT FUNCTIONS

9.3.5.1
A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2
A External WDT "Muzzle" Jumper shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to CPU Command. When the jumper is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3
A WATCHDOG Circuit shall be provided. It shall be enabled by the FIELD I/O software at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4
ONE KHz REFERENCE - A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

9.3.5.5
A 32-bit MILLISECOND COUNTER (MC) shall be provided for "timestamping." Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6
At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.

9.3.5.7
A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled "SP3 ON". If LED lite ON, SP3 is active and available at C12S.

9.3.6*
SERIAL COMMUNICATIONS / LOGIC CIRCUITRY

9.3.6.1*
System Serial Port 5 (SP%) EIA 485 signal Lines shall enter the I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2*
System Serial Port 3 (SP#) EIA 485 signal lines shall enter the I/O module and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3*
LINESYNC and POWER DOWN Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4*
CPU RESET and POWER UP (SYSRESET) Lines shall be isolated and "OR'd" to form NRESET. NRESET shall be used to reset FCU and other module devices. NRESET shall also, be converted to EIA 485, then routed to Connector C12S.

9.3.6.5*
If the module is 2070-2B, routing to FCU doesn't apply.

9.3.6.6*
Isolation is between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

9.3.7
BUFFERS

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

9.3.8
I/O FUNCTIONS

9.3.8.1
INPUTS - Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 μs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 μs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μs of the completion of the input scan.

9.3.8.2
DATA FILTERING - If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The

filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	**Enabled**
On and off filter values shall be set to	**5**
Transition monitoring	**Disabled (Timestamps are not logged)**

9.3.8.3
OUTPUTS - Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4
Standard Function - Each output shall be controlled by the data and control bits in the CPU Module-FI/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	**0**	**0**	**Output in the OFF state**
B	**1**	**1**	**Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.**
C	**0**	**1**	**Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF**
D	**1**	**0**	**Output is in the ON state.**

9.3.8.4.1
In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

9.3.8.5
Interrupts - All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared

only on command. LINESYNC Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds (≥60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).

9.3.8.6
Communication Service Routine - A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

Generate the opening and closing flags
Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero bit insertion

For Receiving:

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

9.3.8.7
Communication Processing - The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

9.3.8.8
Input Processing - This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9
DATA COMMUNICATION PROTOCOLS

9.3.9.1
Protocols - All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

9.3.9.1.1

The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
49	177	Request Module Status	250 µs	275 us
50	178	MILLISECOND CTR. Mgmt.	222.5 µs	237.5 us
51	179	Configure Inputs	344.5 µs	6.8750 ms
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 ms
55	183	Command Outputs	405 µs	410 µs
56	184	Config. Input Tracking Functions	340 µs	10.25 ms
57	185	Config. Complex Output Functions	340 µs	6.875 ms
58	186	Configure Watchdog	222.5 µs	222.5 µs
59	187	Controller Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62	189-190	Reserved (note below)		
63	191	Poll variabl length raw input	317.5 us	320 us
64	192	Variable length command outputs	405 us	410 us

9.3.9.1.2

Message's 61 / 189 and 62 / 190 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (pending TEES Chapter 7). Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of inuts bytes. Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

9.3.9.2

REQUEST MODULE STATUS - The Command shall be used to request FI/O status information response. Command/response frames are as follows:

Request Module Status Command

Description	Msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	Msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

9.3.9.2.1
The response status bits are defined as follows:

P - Indicates FI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the FI/O has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Indicates the Datakey has failed or is not present

9.3.9.2.2
Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3
MC MANAGEMENT frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	msb							Lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	X	x	X	x	x	x	x	Byte 2
New Timestamp NMSB	x	X	x	X	x	x	x	x	Byte 3
New Timestamp NLSB	x	X	x	X	x	x	x	x	Byte 4
New Timestamp LSB	x	X	x	X	x	x	x	x	Byte 5

Millisecond Counter Management Response

Description	msb							Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

9.3.9.4

CONFIGURE INPUTS - The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb							Lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	N	n	N	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	msb							Lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

9.3.9.5

POLL RAW INPUT DATA - The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	msb							lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16

Timestamp MSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 17**
Timestamp NMSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 18**
Timestamp NLSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 19**
Timestamp LSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 20**

9.3.9.6

POLL FILTERED INPUT DATA - The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes(-2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	**Msb**							**lsb**	**Byte Number**
(Type Number = 53)	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**Byte 1**

Poll Filter Input Data Response

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 181)	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**Byte 1**
Inputs I0 (lsb) to I7 (msb)	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 2**
Inputs I8 to I119	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Bytes 3 to 16**
Timestamp MSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 17**
Timestamp NMSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 18**
Timestamp NLSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 19**
Timestamp LSB	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**Byte 20**

9.3.9.7

POLL INPUT TRANSITION BUFFER - The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 54)	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**Byte 1**
Block Number	**x**	**x**	**x**	**X**	**x**	**X**	**x**	**x**	**Byte 2**

Input Transition Buffer Response

Description	msb							lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2
Number of Entries	x	x	x	X	x	X	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
Timestamp MSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+8
Timestamp NMSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+9
Timestamp NLSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+10
Timestamp LSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+11

9.3.9.7.1

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- **S - Indicates the state of the input after the transition**
- **C - Indicates the 255 entry buffer limit has been exceeded**
- **F - Indicates the 1024 buffer limit has been exceeded**
- **G - Indicates the requested block number is out of monotonic increment sequence**
- **E - Same block number requested, E is set in response**

9.3.9.7.2

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8

SET OUTPUTS - The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	X	x	x	X	x	x	x	x	Byte 2
Outputs O8 to O103 Data	X	x	x	X	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	X	x	x	X	x	x	x	x	Byte 15
Outputs O8 to O103 Control	X	x	x	X	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

9.3.9.9

CONFIGURE INPUT TRACKING FUNCTIONS - The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb							lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	X	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	X	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	X	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	X	x	x	x	x	Byte 6

9.3.9.9.1

Definitions are as follows:

E '1' - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.2

The timestamp value shall be sampled prior to the response frame.

9.3.9.9.3

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.4

The "Number of Item" field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message "V" bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10

CONFIGURE COMPLEX OUTPUT FUNCTIONS - The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb							lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	X	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	X	X	x	x	x	Byte 4
Timestamp (NLSB)	x	X	x	X	X	x	x	x	Byte 5
Timestamp (LSB)	x	X	x	X	X	x	x	x	Byte 6

9.3.9.10.1
The bit fields of the command frame are defined as follows:

E '1' - enable complex output function for this output
'0' - disable complex output function for this output
J '1' - During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
'0' - During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.
Output Number - 7-bit output number identifying outputs
Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
'0' - The trigger or gate shall be derived from the raw input.
R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
'0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
Input Number - 7-bit input number identifying inputs 0 Up.
P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
'0' - The output is configured for continuous oscillation.
W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
'0' - Operation shall begin within 2 ms of the command receipt.
G '1' - Operation shall be gated active by the specified input.
'0' - Gating is inactive.
L '1' - The LINESYNC based clock shall be used for the time ticks.
'0' - The MC shall be used for the time ticks.
V '1' - Indicates maximum number of configurable outputs is exceeded.
'0' - No error
Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

9.3.9.10.2
Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.3
The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedenceover the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscilla tion should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11
CONFIGURE WATCHDOG - The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	X	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

9.3.9.11.1
The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.2
On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12

CONTROLLER IDENTIFICATION – This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit "K" shall be set and no interrogation shall take place. If a error occurs during the interrogation, Bit "K" shall be set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	msb							lsb	Byte Number
Type Number= 59	0	0	1	1	1	0	1	1	Byte 1

Controller Identication Response

Description	msb							lsb	Byte Number
Type Number = 187	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Bytes 3 to 130

9.3.9.13

MODULE IDENTIFICATION - The FI/O Identification command frame shall be used to request the FI/O Identification value Response of "1" for the 2070-2A, "2" for the 2070-8 FI/O, and "32 to 40" for ITS Cabinet SIUs and SMU/TMU. The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb							lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	msb							lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O I D byte	x	x	x	X	x	x	x	x	Byte 2

CHAPTER 9 SECTION 4

MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1
The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A - FPA controller, two keyboards, AUX switch, alarm bell & Display A
OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell & Display B
OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60S.

9.4.2
Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3
The cathode of the CPU ACTIVE LED INDICATOR shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

9.4.4
The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with a minimum character dimensions of 5.00 mm wide by 10.44 mm high and an electro -luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high and either LED or EL backlight.

9.4.4.1
Each character shall be composed of a 5 x 7 dot matrix with a underline row or a 5 x 8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90^{o}) viewing, +/-35^{o} vertical, +/-45^{o} horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2
The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3
Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5
The FPA CONTROLLER shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1
A FPA RESET Switch shall be provided on the Assembly PCB. The momentary CONTROL switch shall be logic OR'd with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur:

1. **Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.**
2. **Each special character shall be set to ASCII SPC (space).**
3. **The tab stops shall be set to columns 9, 17, 25, and 33.**
4. **The backlight timeout value shall be set to 6 (60 seconds).**
5. **The backlight shall be extinguished.**
6. **The display shall be cleared (all ASCII SPC).**
7. **The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is " ESC [PU", hex value "1B 5B 50 55".**

9.4.5.2
When a keypress is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3
Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

9.4.5.4
When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

9.4.5.5
The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol on Page 9-7-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6
Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been

overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7
Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8
Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9
Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60 % ON / 40 % OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10
Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

9.4.5.11
Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12
Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13
The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14
The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)

Px: Display column number (1-40), using one ASCII character per digit without leading zero.
Py: Display line (1-4) one ASCII character
...: Continue the list in the same fashion

Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

9.4.5.15
The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

9.4.5.16*
C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6
The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CHAPTER 9 SECTION 5

MODEL 2070-4 POWER SUPPLY MODULE

9.5.1
The Model 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices. The Model 2070-4B Module shall meet the same requirements as the 2070-4A except for 3.5 Amperes of +5 VDC and the +5 VDC STANDBY Power.

9.5.2
An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

9.5.3
INPUT PROTECTION - Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4*
+5 VDC STANDBY POWER shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

9.5.5
MONITOR CIRCUITRY shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1
The ACFAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 ms after ACFAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/- 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

9.5.5.2
The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 *
The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ±1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor

circuit shall compensate for missing pulses and line noise during normal operation.

9.5.5.4
The LINESYNC shall continue until SYSRESET transitions LOW and begin then SYSRESET transitions HIGH.

9.5.6
POWER SUPPLY REQUIREMENTS

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	1.0 AMP	10.0 AMP - MODULE 2070-4A 3.5 AMP – MODULE 2070-4B
+12 VDC Serial	+11.4 to +12.6 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11.4 to –12.6 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.4 to +12.6 VDC	0.1 AMP	1.0 AMP

9.5.6.1 Line / L/oad Regulation - shall meet the table tolerances values for voltage range of 90 to 135 VAC,, minimum and maximum loads called out in the table & including ripple noise.

9.5.6.2 Efficiency - 70 % minimum

9.5.6.3 Ripple & noise - Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater

9.5.6.4 Voltage Overshoot - No greater than 5 %, all outputs

9.5.6.5 Overvoltage Protection - 130% Vout for all outputs

9.5.6.6 Overload & Short - Power foldback point 120% of max rated power
Circuit Protection - Automatic recovery upon removal of fault

9.5.6.7 Inrush Current - Cold Start Inrush shall be less than 25A at 115VAC

9.5.6.8 Transient response - Output voltage back to within 1% in less than 500 μs on a 50% Load change. Peak transient not to exceed 5%

9.5.6.9 Holdup Time - The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period

9.5.6.10 Remote Sense - +5 VDC compensates 250 mV total line drop. Open sense load protection required

CHAPTER 9 SECTION 6

UNIT CHASSIS AND MODEL 2070-5 VME CAGE ASSEMBLY

9.6.1
GENERAL - The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2*
SERIAL MOTHERBOARD shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the MOTHERBOARD PCB (provide strain relief). Test points shall be provided on the FPA side of the MOTHERBOARD for PS2 lines. A wiring harness FP shall be provided, linking the MOTHERBOARD with the FPA.

9.6.3
MODEL 2070-5 VME CAGE ASSEMBLY shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24: D16 Interface.

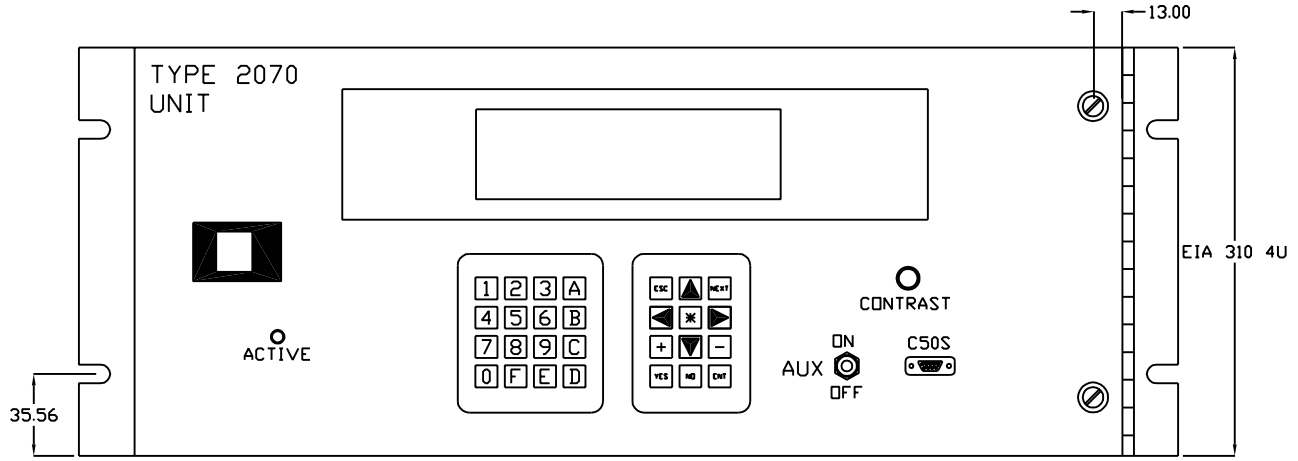
9.6.4
The Model 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

CHAPTER 9 SECTION 7

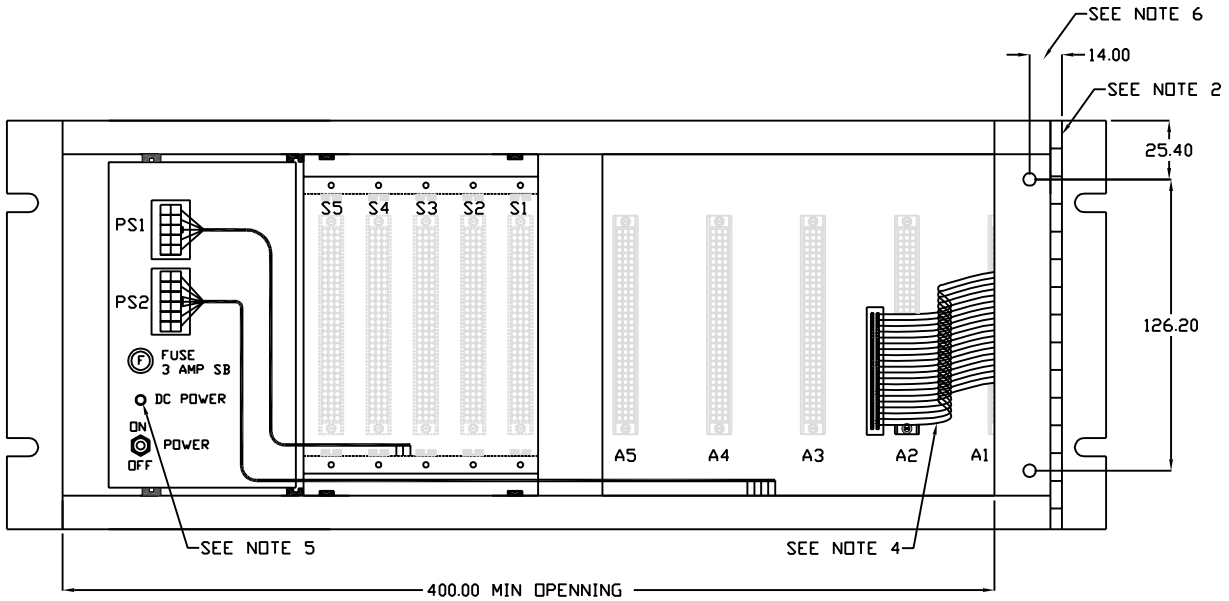
CHAPTER DETAILS

TABLE OF CONTENTS

All dimensions are in millimeters.



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (4 mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

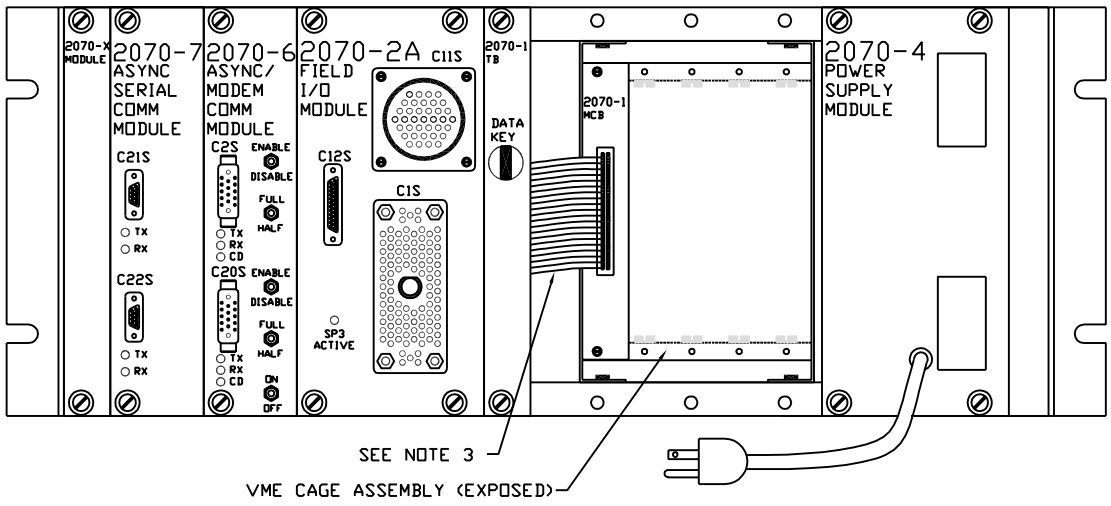
3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

4. The length of the Front Panel Harness shall be no less than 284 mm.

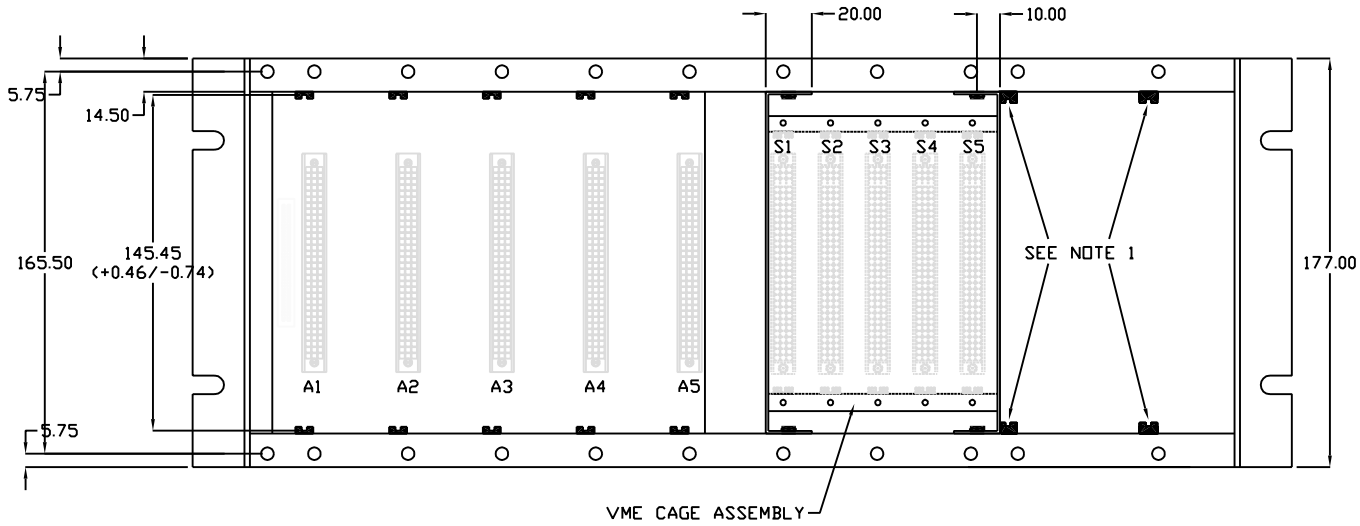
5. A LED indicator for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside panel) shall be 14.00 mm.

	TITLE: TYPE 2070 CHASSIS FRONT VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	9-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

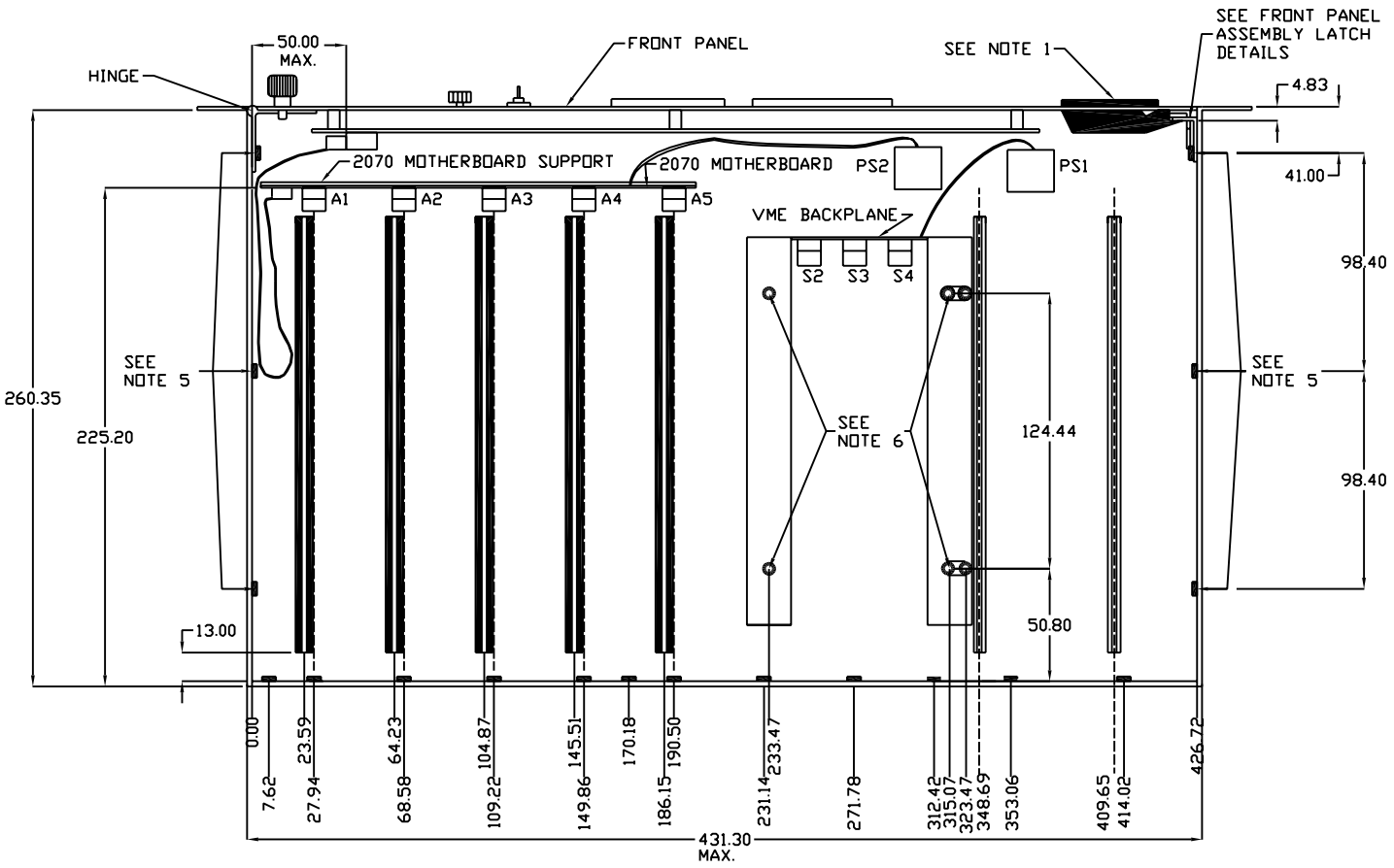
1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

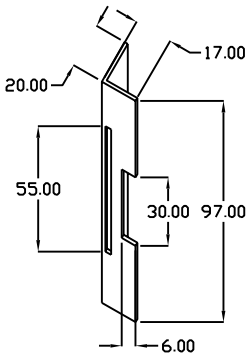
2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

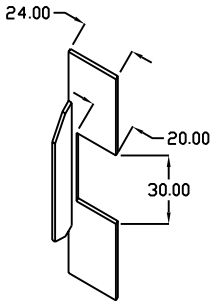
4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

	TITLE: TYPE 2070 CHASSIS REAR VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	9-7-2

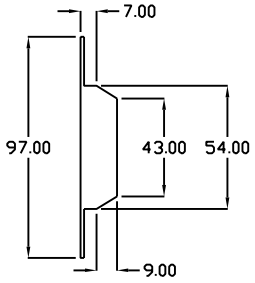




CHASSIS BRACKET



FRONT PANEL BRACKET



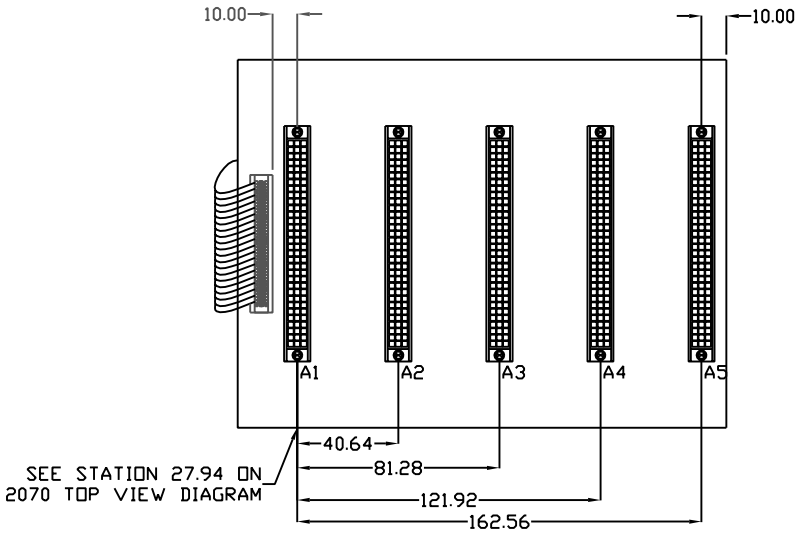
SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

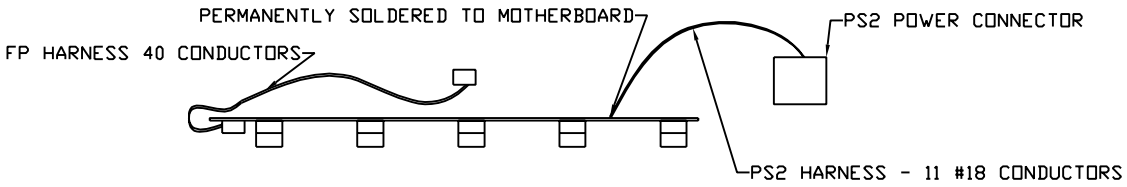
NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 25 mm when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Type 2070-8 Module. Fastener centers shall be 6.35 mm above unit baseline.
6. Eight 6-32 Phillips head screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

TITLE:	TYPE 2070 CHASSIS TOP VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	9-7-3



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	C50 ENABLE
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The location of the FP Harness on either side of the motherboard is allowed. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE:

TYPE 2070 CHASSIS MOTHERBOARD

	NO SCALE	
	TEES, NOV 19, 1999	9-7-4

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCO+	SP5RXD+
6	SP3RTS-	SP3TXCO-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCO+
20	NA	NA	SP3TXCO-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCG #1	(SEE NOTE 4)	SP3TXCI+
22	NETWK1	(SEE NOTE 4)	SP3TXCI-
23	NETWK2	(SEE NOTE 4)	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial. DC GND #2 for +12VDC ISO.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".

   Connector A2, pin B23 shall read "A2 Installed".

   Connector A3, pin B23 shall read "A3 Installed".

   Connector A4, pin B23 shall read "NA".

   Connector A5, pin B21 shall read "A2 Installed".

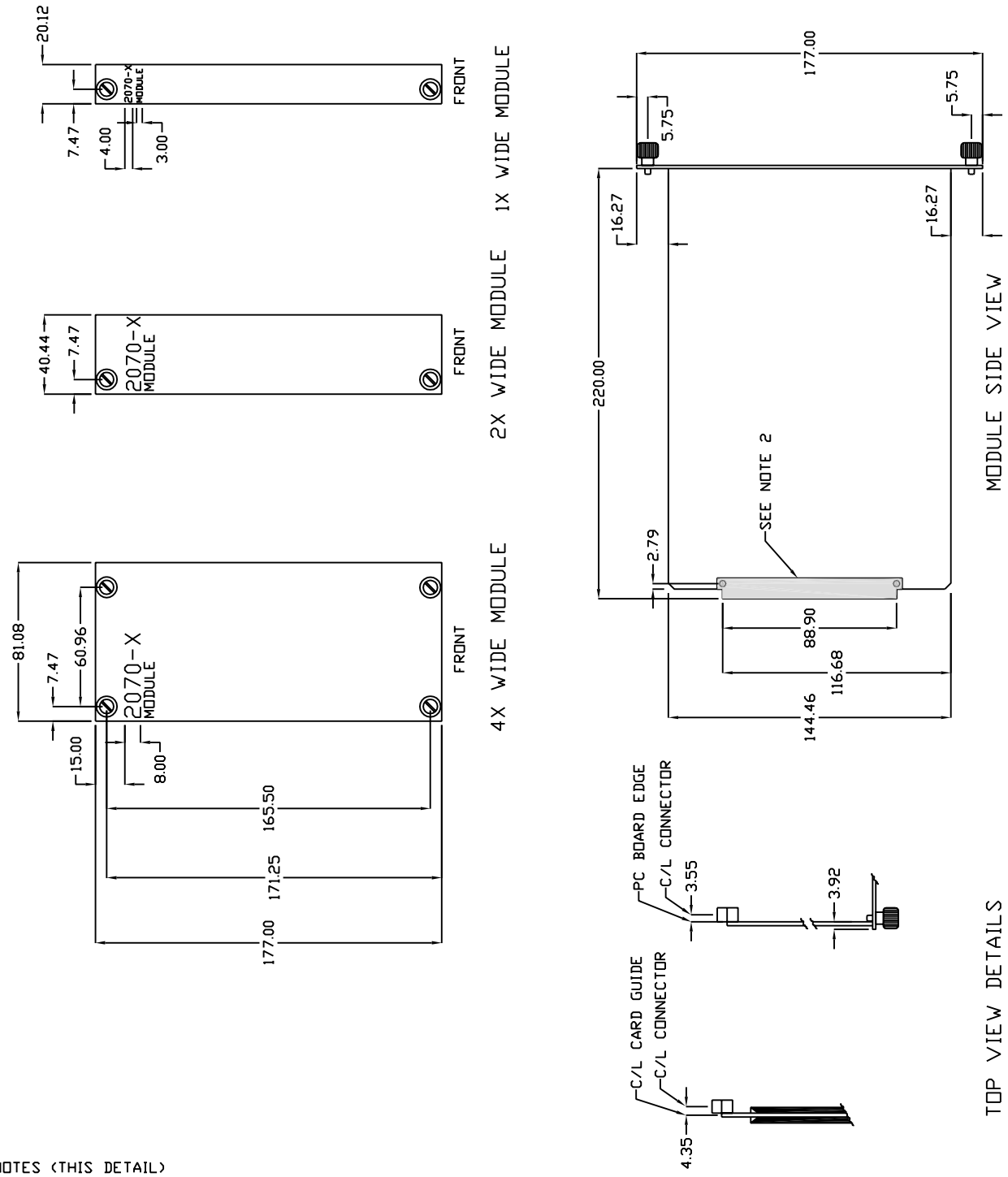
   Connector A5, pin B22 shall read "DCG #1".

   Connector A5, pin B23 shall read "A3 Installed".
5. Pin A24 (DCG #1) is reserved for network protection only, ie., "Ethernet Shield".
6. Connector A2 installed, enables SP1 and SP2.
7. Connector A3 installed, enables SP5.
8. SP3 and SP6 are always enabled.
9. C50 enabled, disconnects SP4 on connector A1.

TITLE:

Motherboard A Connector Pin Assignment

	NO SCALE	
	TEES, NOV 19, 1999	9-7-5



NOTES (THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL.

2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

TITLE:

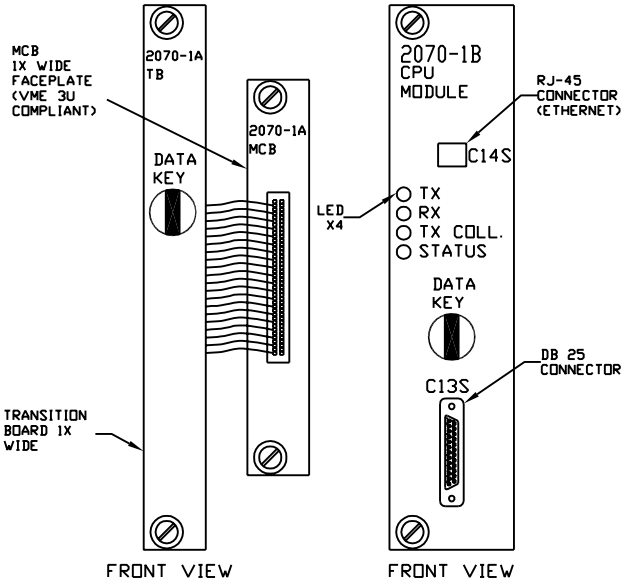
TYPE 2070 SYSTEM PCB MODULES, GENERAL

NO SCALE	
TEES, NOV 19, 1999	9-7-6a

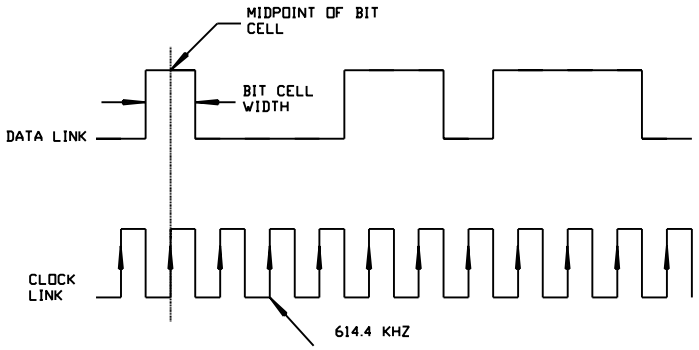
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1)	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4

2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6

3. * Default BPS Rate for indicated Port.
   ** Disconnected by internal switch.

4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF THE 2070-1B is Dual SCC1 with 68360 SCC1 assigned to ETHERNET.

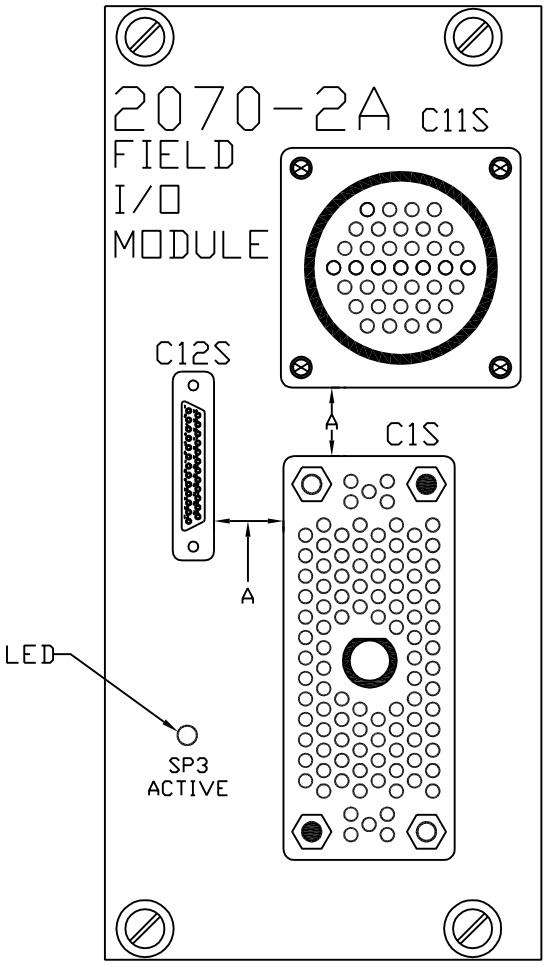
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

TITLE: TYPE 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL

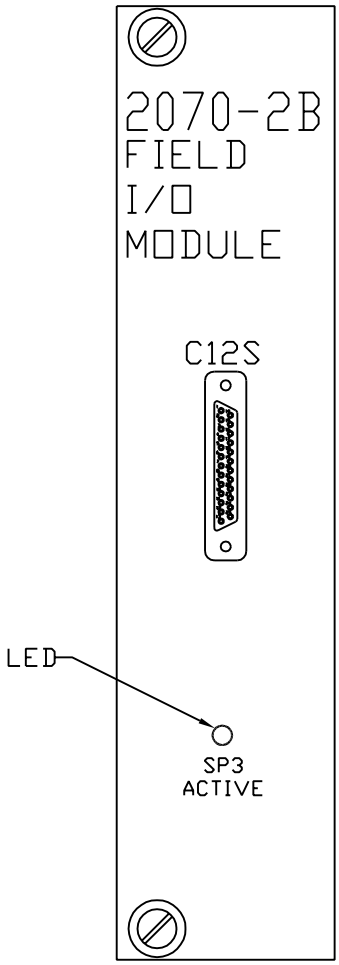
NO SCALE

TEES, NOV 19, 1999

9-7-7



FRONT VIEW



FRONT VIEW

FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

5. C12S Pin 12 +5 VDC is derived from the +12 VDC power supply.

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

TYPE 2070-2
FIELD I/O MODULES

	NO SCALE	
	TEES, NOV 19, 1999	9-7-8

C1S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	DC GROUND	
2	O0	O1-1
3	O1	O1-2
4	O2	O1-3
5	O3	O1-4
6	O4	O1-5
7	O5	O1-6
8	O6	O1-7
9	O7	O1-8
10	O8	O2-1
11	O9	O2-2
12	O10	O2-3
13	O11	O2-4
14	DC GROUND	
15	O12	O2-5
16	O13	O2-6
17	O14	O2-7
18	O15	O2-8
19	O16	O3-1
20	O17	O3-2
21	O18	O3-3
22	O19	O3-4
23	O20	O3-5
24	O21	O3-6
25	O22	O3-7
26	O23	O3-8

PIN	FUNCTION	
	NAME	PORT
27	O24	O4-1
28	O25	O4-2
29	O26	O4-3
30	O27	O4-4
31	O28	O4-5
32	O29	O4-6
33	O30	O4-7
34	O31	O4-8
35	O32	O5-1
36	O33	O5-2
37	O34	O5-3
38	O35	O5-4
39	I0	I1-1
40	I1	I1-2
41	I2	I1-3
42	I3	I1-4
43	I4	I1-5
44	I5	I1-6
45	I6	I1-7
46	I7	I1-8
47	I8	I2-1
48	I9	I2-2
49	I10	I2-3
50	I11	I2-4
51	I12	I2-5
52	I13	I2-6

PIN	FUNCTION	
	NAME	PORT
53	I14	I2-7
54	I15	I2-8
55	I16	I3-1
56	I17	I3-2
57	I18	I3-3
58	I19	I3-4
59	I20	I3-5
60	I21	I3-6
61	I22	I3-7
62	I23	I3-8
63	I28	I4-5
64	I29	I4-6
65	I30	I4-7
66	I31	I4-8
67	I32	I5-1
68	I33	I5-2
69	I34	I5-3
70	I35	I5-4
71	I36	I5-5
72	I37	I5-6
73	I38	I5-7
74	I39	I5-8
75	I40	I6-1
76	I41	I6-2
77	I42	I6-3
78	I43	I6-4

PIN	FUNCTION	
	NAME	PORT
79	I44	I6-5
80	I45	I6-6
81	I46	I6-7
82	I47	I6-8
83	O40	O6-1
84	O41	O6-2
85	O42	O6-3
86	O43	O6-4
87	O44	O6-5
88	O45	O6-6
89	O46	O6-7
90	O47	O6-8
91	O48	O7-1
92	DC GROUND	
93	O49	O7-2
94	O50	O7-3
95	O51	O7-4
96	O52	O7-5
97	O53	O7-6
98	O54	O7-7
99	O55	O7-8
100	O36	O5-5
101	O37	O5-6
102	O38 DET RES	O5-7
103	O39 WDT	O5-8
104	DC GROUND	

C11S PIN ASSIGNMENT

PIN	FUNCTION	
	NAME	PORT
1	O56	O8-1
2	O57	O8-2
3	O58	O8-3
4	O59	O8-4
5	O60	O8-5
6	O61	O8-6
7	O62	O8-7
8	O63	O8-8
9	DC GROUND	
10	I24	I4-1

PIN	FUNCTION	
	NAME	PORT
11	I25	I4-2
12	I26	I4-3
13	I27	I4-4
14	DC GROUND	
15	I48	I7-1
16	I49	I7-2
17	I50	I7-3
18	I51	I7-4
19	I52	I7-5
20	I53	I7-6

PIN	FUNCTION	
	NAME	PORT
21	I54	I7-7
22	I55	I7-8
23	I56	I8-1
24	I57	I8-2
25	I58	I8-3
26	I59	I8-4
27	I60	I8-5
28	I61	I8-6
29	I62	I8-7
30	I63	I8-8

PIN	FUNCTION	
	NAME	PORT
31	DC GROUND	
32	NA	- - -
33	NA	- - -
34	NA	- - -
35	NA	- - -
36	NA	- - -
37	DC GROUND	

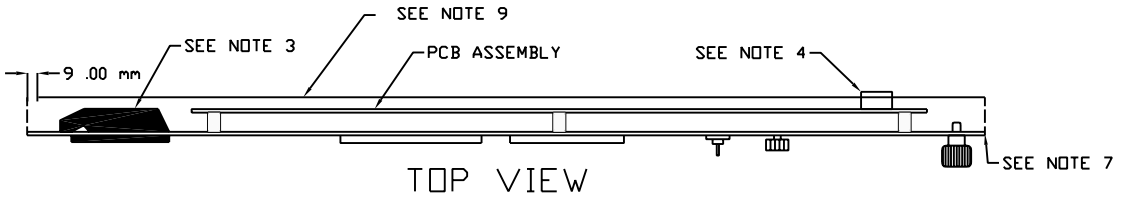
TITLE:

TYPE 2070-2A
FIELD I/O MODULE
C1 & C11 CONNECTORS

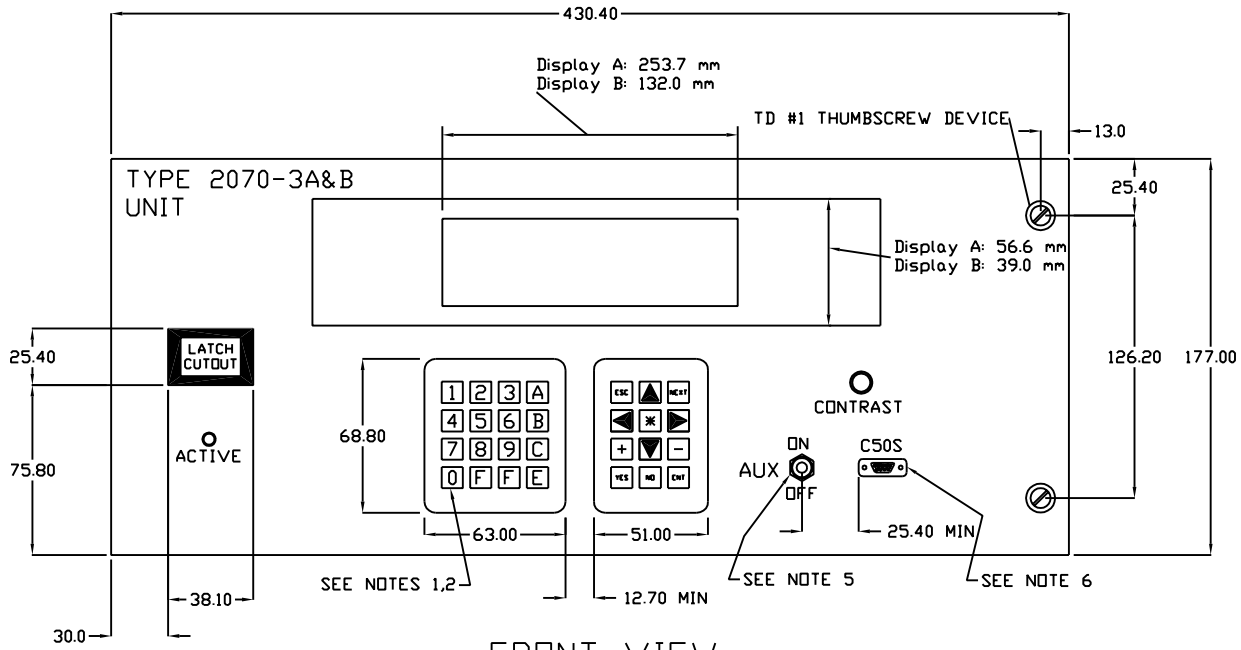
NO SCALE

TEES, NOV 19, 1999

9-7-9



TOP VIEW



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. The center of the FP Harness Pin Header shall be vertically positioned between 85 and 95 mm as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Fron panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 - ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60S CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TITLE:

TYPE 2070-3A&B FRONT PANEL ASSEMBLY

NO SCALE	
TEES, NOV 19, 1999	9-7-10

TYPE 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

TYPE 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE:

TYPE 2070-3 FRONT PANEL ASSEMBLY KEY CODES

NO SCALE

TEES, NOV 19, 1999

9-7-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on (Note 2)
ESC [27 l	1B 5B 32 37 6C	Reverse video off (Note 2)
ESC [24 h	1B 5B 32 34 68	Underline on (Note 2)
ESC [24 l	1B 5B 32 34 6C	Underline off (Note 2)
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A. Reverse Video is NOT required for Option 3B. Command codes shall be avaliable for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

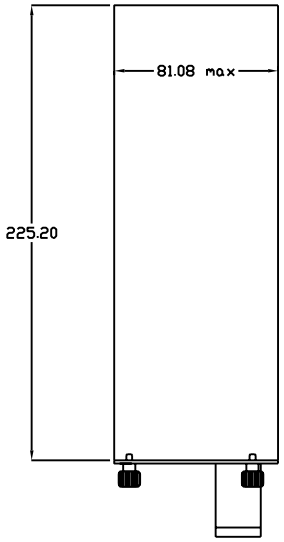
COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE:
TYPE 2070-3 FRONT PANEL ASSEMBLY KEY CODES

NO SCALE

TEES, NOV 19, 1999

9-7-12



TOP VIEW

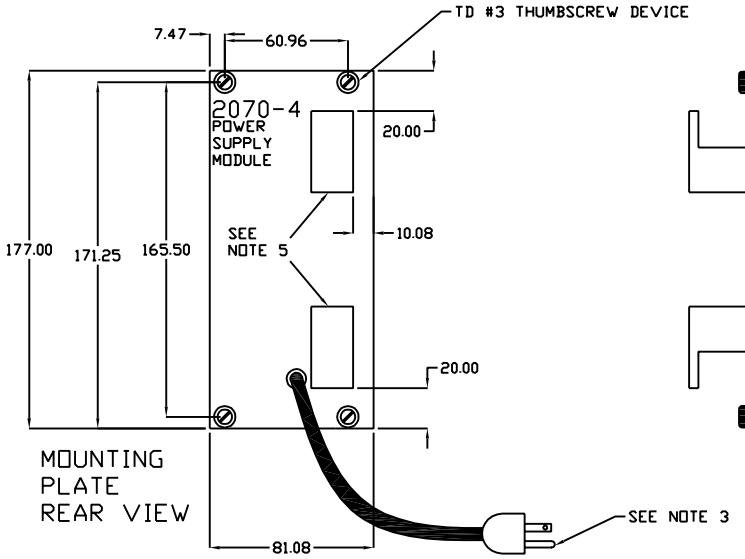
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC
7	DC GROUND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

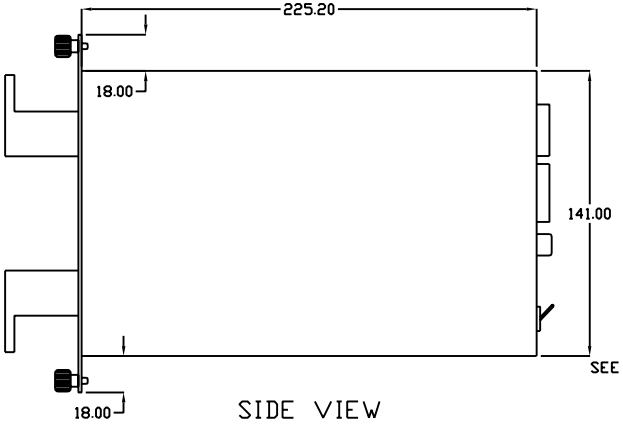
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

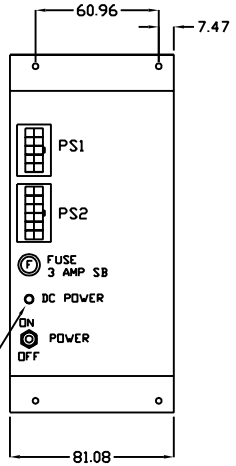
   PS1 connector shall be a 10 position PLUG connector. PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, +12 ISO, +12 SER, and -12 SER).



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



FRONT VIEW

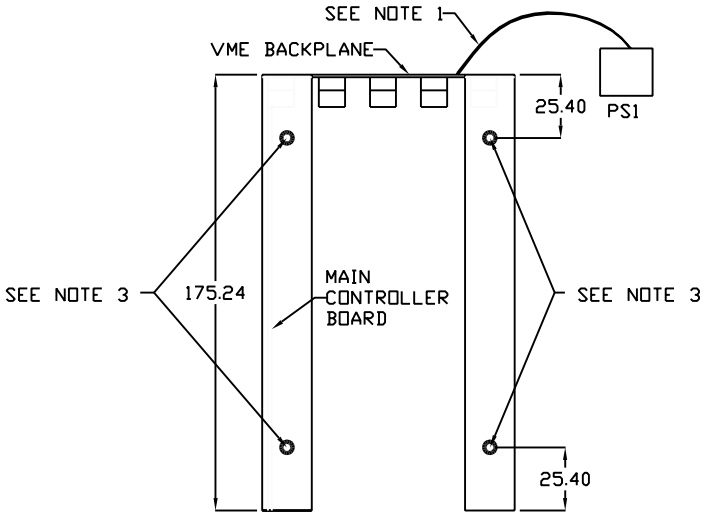
TITLE:

TYPE 2070-4
POWER SUPPLY MODULE

NO SCALE

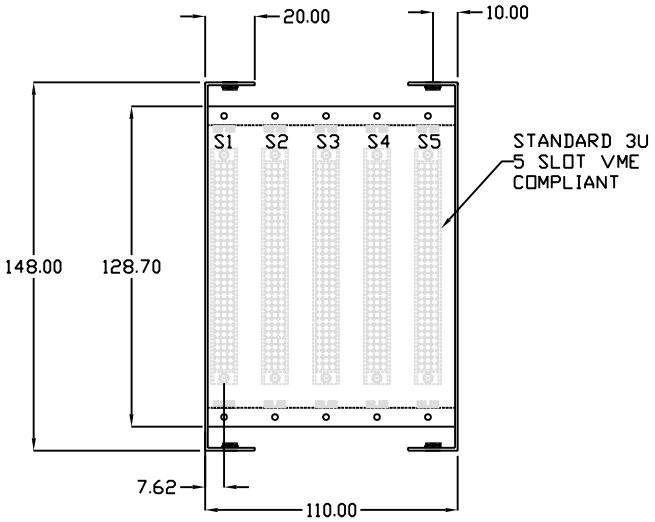
TEES, NOV 19, 1999

9-7-13a



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Type 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area and attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Type 2070 Chassis Top View Detail.

3. 6-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 Phillips screws on the top and bottom of the Type 2070 chassis.

TITLE:

TYPE 2070-5
VME CAGE ASSEMBLY

NO SCALE	
TEES, NOV 19, 1999	9-7-14

CHAPTER 10

SPECIFICATION FOR MODEL 2070 PERIPHERAL EQUIPMENT AND THE MODEL 2070N CONTROLLER UNIT

TABLE OF CONTENTS

GENERAL NOTES:

1. **The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). The Disable line shall be pulled up on the module.**
2. **Line drivers/receivers shall be socket mounted.**
3. **Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.**
4. **The Comm modules shall be "Hot" swappable without damage to circuitry or operations.**

CHAPTER 10 SECTION 1

MODEL 2070-6 A & B ASYNC/MODEM SERIAL COMM MODULES

10.1.1
A fused isolated +5 VDC with a minimum of 100 mA power supply shall be provided for external use.

10.1.2
Three LOGIC switches per circuit shall be provided (faceplate mounted).

10.1.2.1
One shall be used to vertically switch between Half Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.1.2.2
A MODEM ENABLE switch shall be provided that when in UP Position shall enable the MODEM and in DOWN Position disable it.

10.1.2.3
A CONTROL switch shall be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.

10.1.3
Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector). The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

10.1.3.1
Each CIRCUIT shall have a MODEM with the following requirements:

1. **Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.**
2. **Modulation: Phase coherent frequency shift keying (FSK).**
3. **Data Format: Asynchronous, serial by bit.**
4. **Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive):2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, ±1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.**
5. **Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.**
6. **Receiver Input Sensitivity: 0 to -40 dB.**
7. **Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.**
8. *** Clear-to-Send (CTS) Delay: 11 ±3 ms.**
9. **Receive Line Signal Detect Time: 8 ±2 ms mark frequency.**
10. **Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).**

11.* Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for 2070-6B). Whenthe RTS is unasserted , the carrier shall turn off or go to soft carrier frequency.

12. Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

13. Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.

14. Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.

15. Modem interface: EIA-232 Standards.

CHAPTER 10 SECTION 2

MODEL 2070-7A & 7B ASYNC SERIAL COMM MODULE

10.2.1
Two circuits designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

10.2.2
2070 -7A Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.2.3
2070 - 7B Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.2.4
Each circuit signal TX and RX line shall have an LED Indicator mounted on the frontplate and labeled to function.

CHAPTER 10 SECTION 3

MODEL 2070-2A FIELD I/O MODULE

10.3.1
The Model 2070-2A Module shall be a 2X wide PCB Type.

10.3.2
The C12S Connector shall be mounted on the module front panel. The connector type shall be a DB-25 socket connector with pin assignments as follows:

PIN	FUNCTION	PIN	FUNCTION
1	TX DATA+	14	TX DATA-
2	DC GROUND #2	15	DC GROUND #2
3	TX CLOCK+	16	TX CLOCK-
4	DC GROUND #2	17	DC GROUND #2
5	RX DATA+	18	RX DATA-
6	DC GROUND #2	19	DC GROUND #2
7	RX CLOCK+	20	RX CLOCK-
8	LINESYNC+	21	LINESYNC-
9	POWER UP+	22	POWER UP-
10	POWER DOWN+	23	POWER DOWN-
11	NA	24	NA
12	NA	25	EQUIP GND
13	NA		

10.3.3
The module's functions are to isolate (Chapter 9 Section 3 Isolation Specification applies) the EIA-485 internal signal line voltages between the CPU Module and external equipment, and drive/receive interface between said devices. The line drivers/receivers shall be capable of interfacing and operating with external devices up to 1,000 meters away. The line drivers/receivers shall be CMOS devices and socket mounted.

CHAPTER 10 SECTION 4

MODEL 2070N CONTROLLER UNIT

10.4.1
GENERAL

10.4.1.1
The Model 2070-8 NEMA Interface Module Chassis and 2070N Back Cover shall be made of 1.524 mm minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

10.4.1.2
A permanent label shall be affixed to the Model 2070-8 Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

10.4.2
MODEL 2070-8 NEMA INTERFACE MODULE

10.4.2.1
The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors.

10.4.2.2
The Module Front Panel shall be furnished with the following:

1. **ON/OFF POWER Switch mounted vertically with ON in the UP position.**
2. **LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.**
3. **Incoming VAC fuse protection.**
4. **Two DB-25S COMM connectors labeled "EX1" & "EX2."**
5. **Four NEMA Connectors A, B, C, & D.**

10.4.2.3
A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

10.4.2.3.1
Specification 9.5.3 INPUT PROTECTION

10.4.2.3.2*
Specification 9.5.6 POWER SUPPLY REQUIREMENTS except Spec 9.5.3.

10.4.2.3.3
DC Voltage tolerances shall be ±3 %.

10.4.2.4
The supplied incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN."

10.4.2.5
AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

10.4.2.6
A MODULE PC Boards shall be mounted vertically.

10.4.2.7*
Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector. The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.

10.4.2.8
The Model 2070-8 NEMA Interface Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

10.4.2.8.1
PARALLEL PORTS - 118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12 and Ground False, "0," exceeds 16.0 VDC. LINESYNC signal is incoming in differential logic.

10.4.2.8.2
SERIAL COMMUNICATION CIRCUITRY - The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. All signal lines shall be isolated. HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector. All necessary driver/receiver and isolation circuitry shall be provided.

10.4.2.9
An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector.

10.4.2.10
A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.

10.4.2.11
FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 and TS2 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.

10.4.2.11.1
Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.

10.4.2.11.2
The FCU Port 10, Bit 7 output shall normally change its state every 100 ms. A MODULE Watchdog (WDT) circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

10.4.2.11.3
The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

10.4.2.11.4
The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

10.4.2.11.5
CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

10.4.2.11.6
CPU / FCU operation at POWER UP shall be as follows:

1. **FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.**
2. **CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responses to CPU with "E" bit set.**
3. **Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.**
4. *** If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.**
5. **This is operational and preceded User Software.**

10.4.2.11.7
A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in FALSE state.

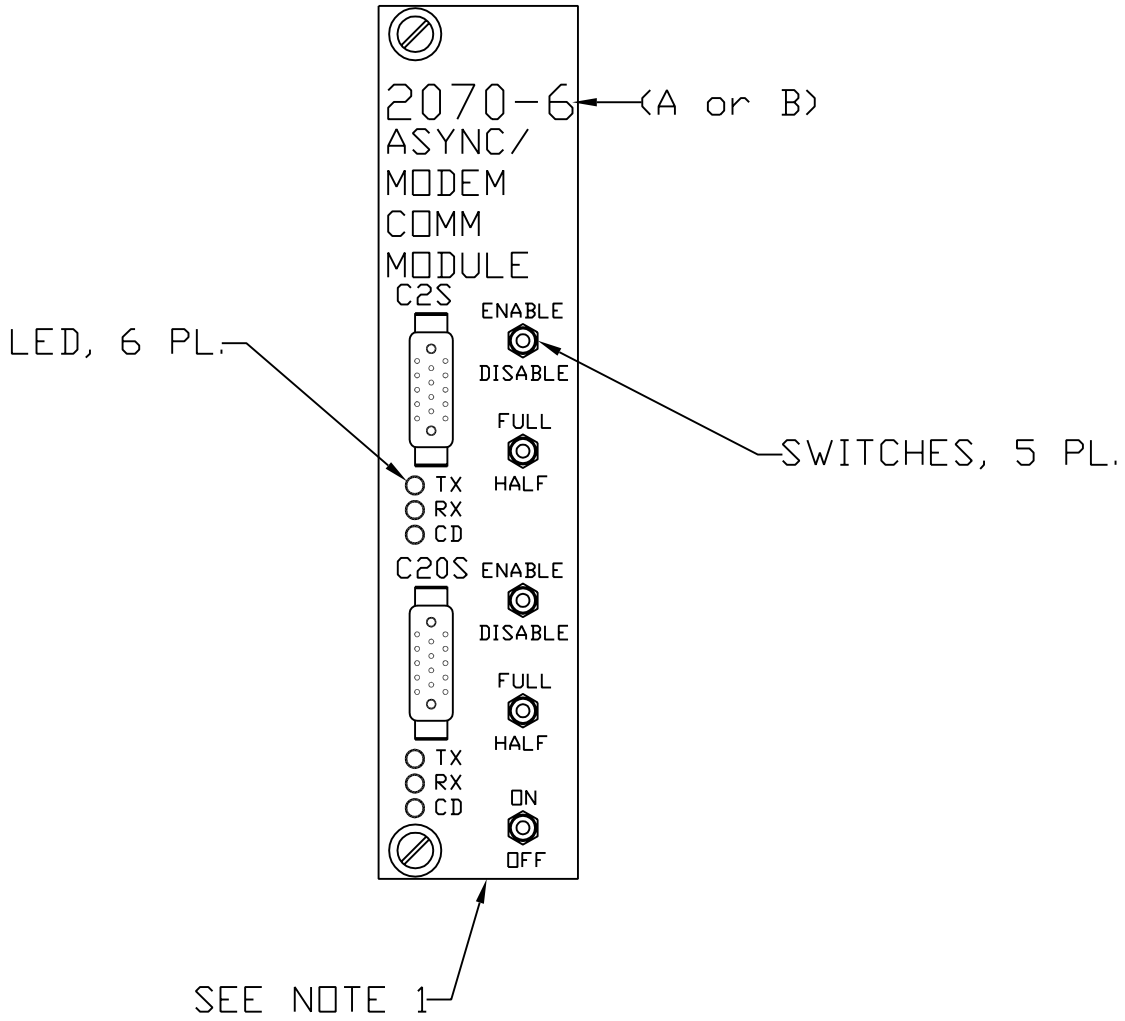
10.4.3
The 2070N Back Cover shall be provided to protect the interface harnesses. The Back Cover shall be delivered attached to the 2070 ATMS Controller Unit and 2070-8 NEMA Interface Module per Section 5.

CHAPTER 10 SECTION 5

CHAPTER DETAILS

TABLE OF CONTENTS

Section Notes:
All dimensions are in millimeters.
Module sheet metal tolerance shall be 0.38 mm or less.



C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

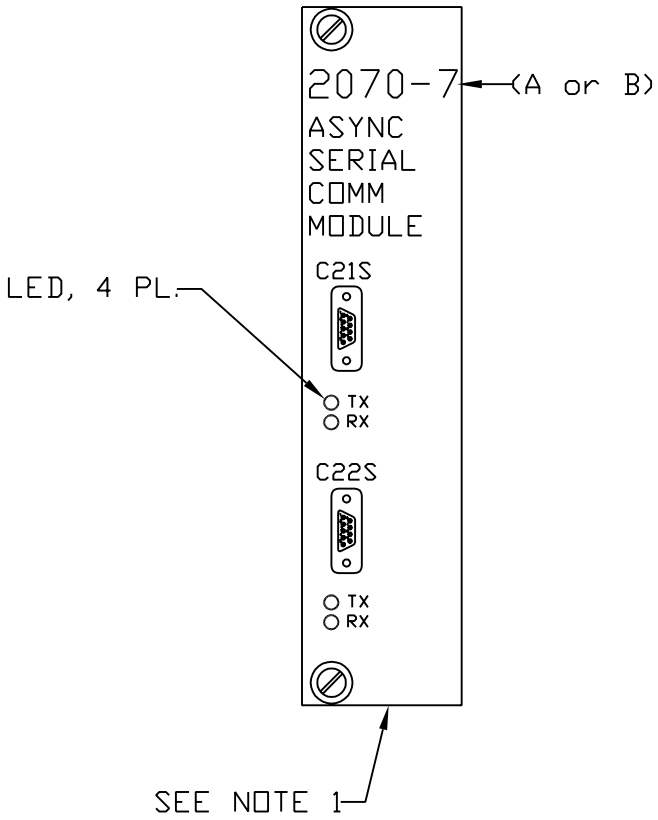
2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

TITLE: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE

NO SCALE

TEES, NOV 19, 1999

10-5-1



2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

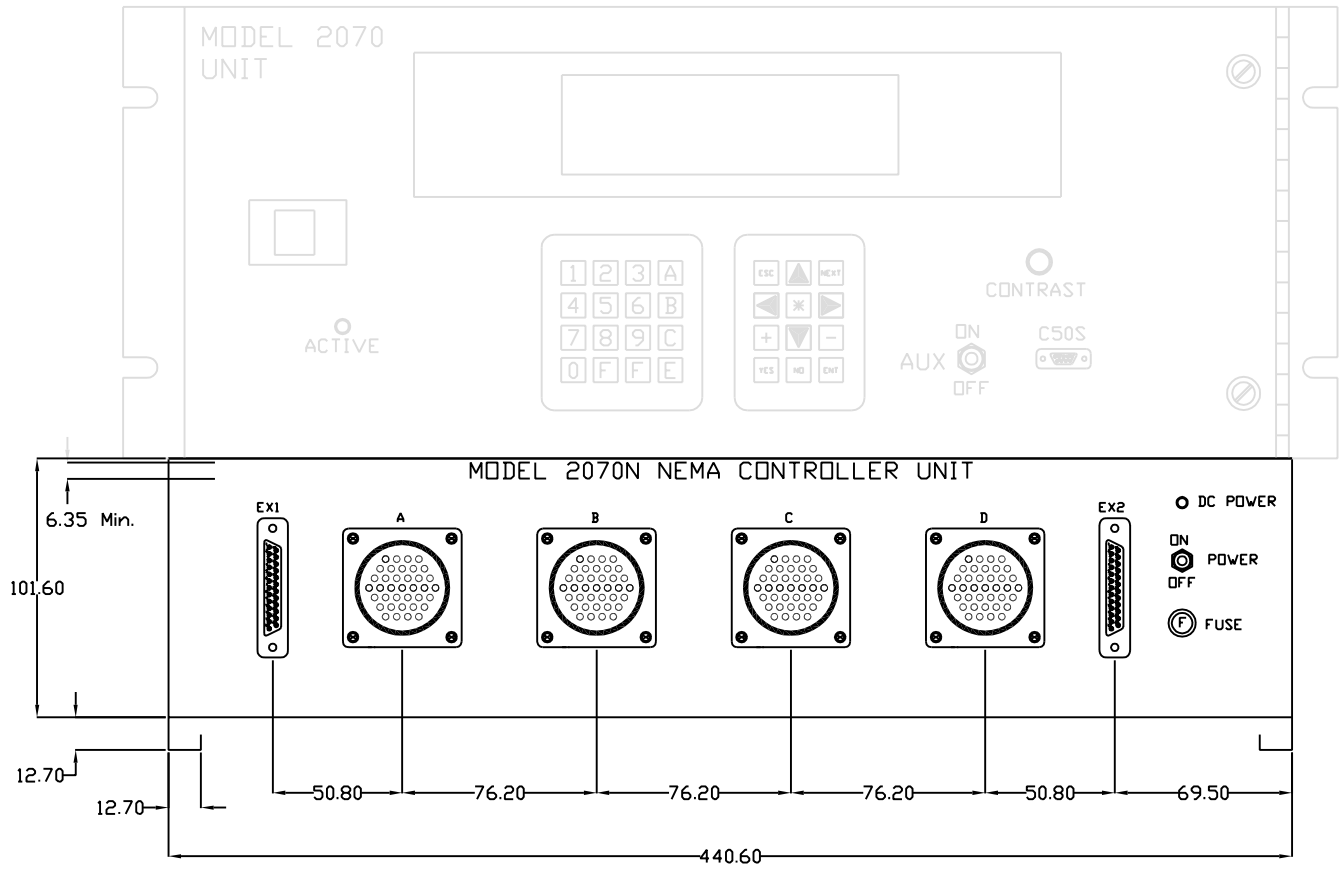
2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

TITLE:
MODEL 2070-7A, 7B
SERIAL COMM MODULE

	NO SCALE	
	TEES, NOV 19, 1999	10-5-2



NOTES (THIS DETAIL)

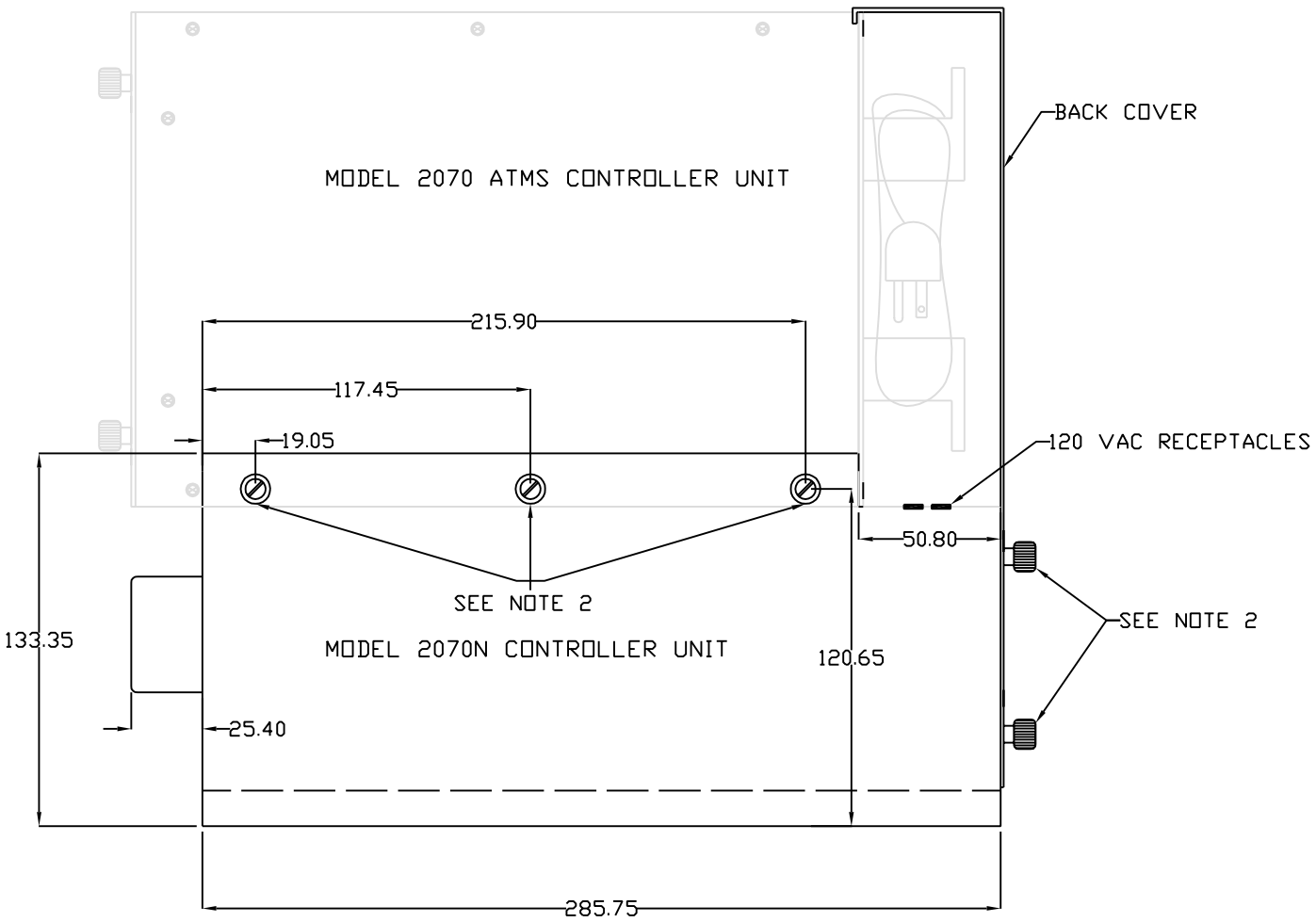
1. The Model 2070 Controller Unit is shown only for refernce.

2. The bottom supports shall be double flanged.

3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)

4. 2.286 mm wide spacers shall be provided between the inside wall of the 2070-8 Module and the 2070 unit (each side).

	TITLE: 2070N CONTROLLER UNIT FRONT VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	10-5-3

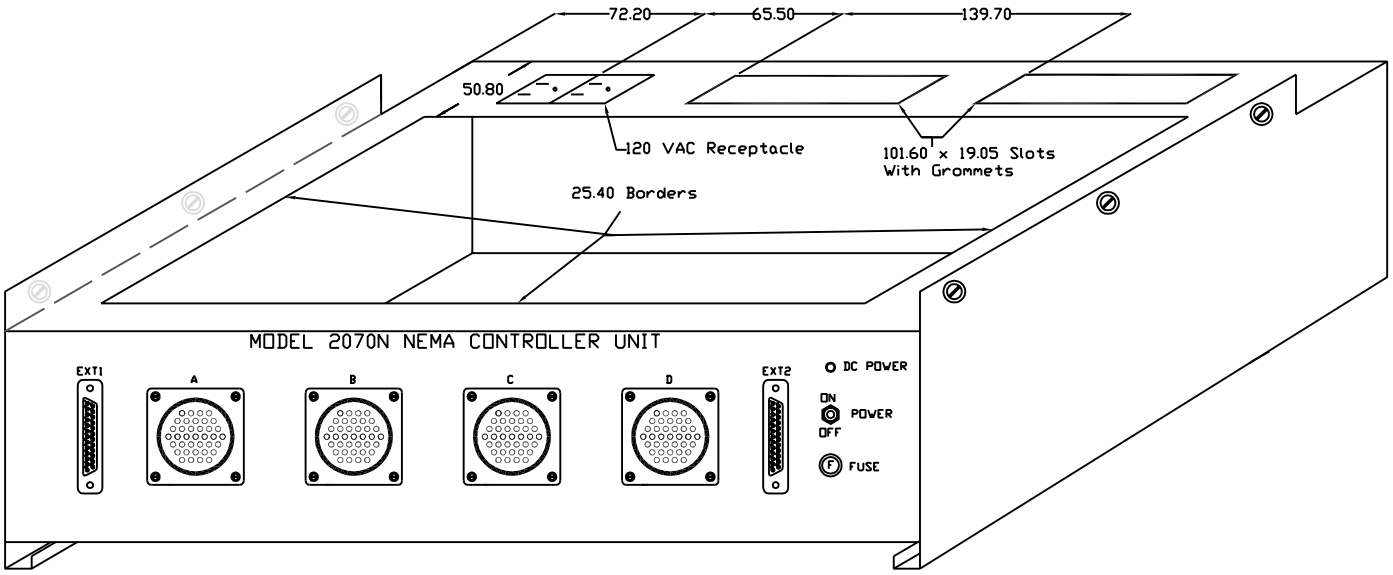


NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.

2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.

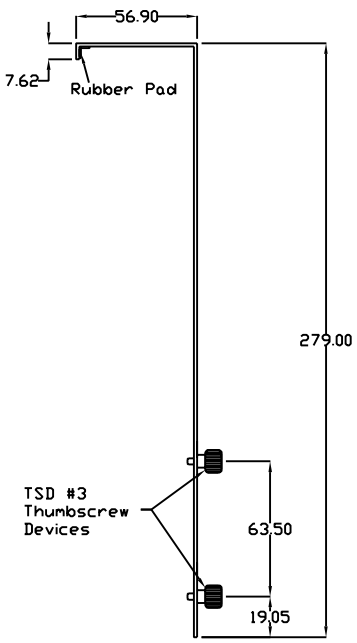
	TITLE: 2070N CONTROLLER UNIT SIDE VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	10-5-4



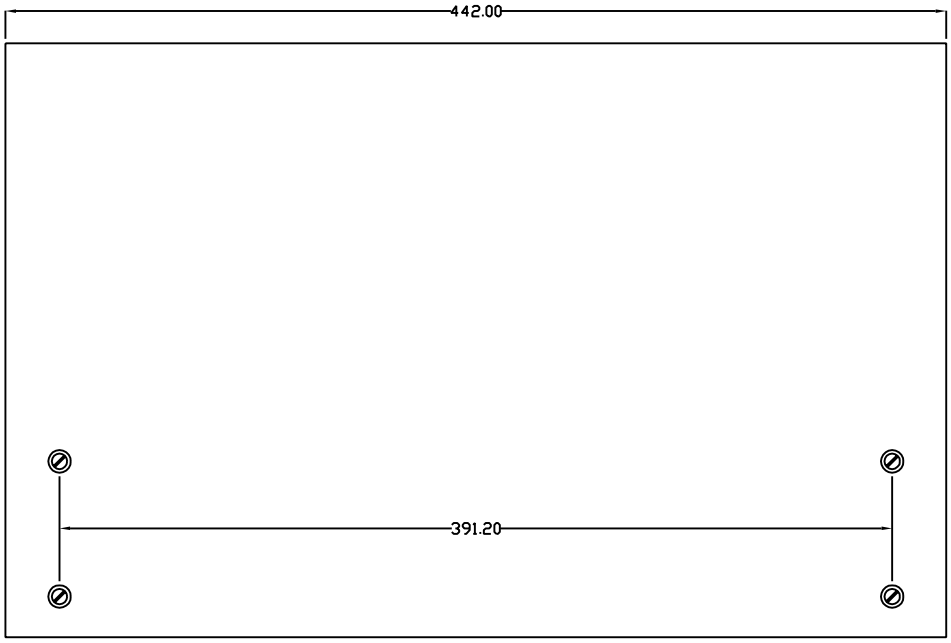
NOTES (THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

	TITLE: 2070N CONTROLLER UNIT ISOMETRIC VIEW	
	NO SCALE	
	TEES, NOV 19, 1999	10-5-5



SIDE VIEW



REAR VIEW

NOTES (THIS DETAIL)

1. The overhang lip shall be notched 19.05 mm on each side.

	TITLE: 2070N CONTROLLER UNIT BACK COVER	
	NO SCALE	
	TEES, NOV 19, 1999	10-5-6

	CONNECTOR A			CONNECTOR B		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Fault Monitor	---	---	Phase 1 Next	Out	8-1
B	+24 VDC External	---	---	Reserved	In	9-5
C	Voltage Monitor	---	---	Phase 2 Next	Out	8-2
D	Phase 1 Red	Out	1-1	Phase 3 Green	Out	3-3
E	Phase 1 Don't Walk	Out	4-1	Phase 3 Yellow	Out	2-3
F	Phase 2 Red	Out	1-2	Phase 3 Red	Out	1-3
G	Phase 2 Don't Walk	Out	4-2	Phase 4 Red	Out	1-4
H	Phase 2 Ped Clear	Out	5-2	Phase 4 Ped Clear	Out	5-4
J	Phase 2 Walk	Out	6-2	Phase 4 Don't Walk	Out	4-4
K	Phase 2 Vehicle Detector	In	1-2	Phase 4 Check	Out	7-4
L	Phase 2 Pedestrian Detector	In	2-2	Phase 4 Vehicle Detector	In	1-4
M	Phase 2 Hold	In	3-2	Phase 4 Pedestrian Detector	In	2-4
N	Stop Timing (Ring 1)	In	6-2	Phase 3 Vehicle Detector	In	1-3
P	Inh Max Term (Ring 1)	In	6-3	Phase 3 Pedestrian Detector	In	2-3
R	External Start	In	8-1	Phase 3 Omit	In	5-3
S	Interval Advance	In	8-2	Phase 2 Omit	In	5-2
T	Indicator Lamp Control	In	8-3	Phase 5 Ped Omit	In	4-5
U	AC Neutral	---	---	Phase 1 Omit	In	5-1
V	Chassis Ground	---	---	Ped Recycle (Ring 2)	In	7-5
W	2070N DC Ground	---	---	Reserved	In	9-6
X	Flashing Logic Out	Out	11-7	Reserved	In	9-7
Y	Coded Status Bit C (Ring 1)	Out	12-3	Phase 3 Walk	Out	6-3
Z	Phase 1 Yellow	Out	2-1	Phase 3 Ped Clear	Out	5-3
a	Phase 1 Ped Clear	Out	5-1	Phase 3 Don't Walk	Out	4-3
b	Phase 2 Yellow	Out	2-2	Phase 4 Green	Out	3-4
c	Phase 2 Green	Out	3-2	Phase 4 Yellow	Out	2-4
d	Phase 2 Check	Out	7-2	Phase 4 Walk	Out	6-4
e	Phase 2 On	Out	9-2	Phase 4 On	Out	9-4
f	Phase 1 Vehicle Detector	In	1-1	Phase 4 Next	Out	8-4
g	Phase 1 Pedestrian Detector	In	2-1	Phase 4 Omit	In	5-4
h	Phase 1 Hold	In	3-1	Phase 4 Hold	In	3-4
i	Force Off (Ring 1)	In	6-1	Phase 3 Hold	In	3-3
j	Min Recall All Phases	In	8-4	Phase 3 Ped Omit	In	4-3
k	Manual Control Enable	In	8-5	Phase 6 Ped Omit	In	4-6
m	Call To Non-Actuated I	In	6-8	Phase 7 Ped Omit	In	4-7
n	Test Input A	In	9-1	Phase 8 Ped Omit	In	4-8
p	AC Power	---	---	Overlap A Yellow	Out	10-2
q	I/O Mode Bit A	In	8-6	Overlap A Red	Out	10-3
r	Coded Status Bit B (Ring 1)	Out	12-2	Phase 3 Check	Out	7-3
s	Phase 1 Green	Out	3-1	Phase 3 On	Out	9-3
t	Phase 1 Walk	Out	6-1	Phase 3 Next	Out	8-3
u	Phase 1 Check	Out	7-1	Overlap D Red	Out	11-6
v	Phase 2 Ped Omit	In	4-2	Reserved	In	9-8
w	Omit All-Red Clear (Phase 1)	In	6-7	Overlap D Green	Out	11-4
x	Red Rest Mode (Ring 1)	In	6-4	Phase 4 Ped Omit	In	4-4
y	I/O Mode Bit B	In	8-7	Not Assigned	---	---
z	Call To Non-Actuated II	In	7-8	Max II Selection (Ring 2)	In	7-6
AA	Test Input B	In	9-2	Overlap A Green	Out	10-1
BB	Walk Rest Modifier	In	9-4	Overlap B Yellow	Out	10-5
CC	Coded Status Bit A (Ring 1)	Out	12-1	Overlap B Red	Out	10-6
DD	Phase 1 On	Out	9-1	Overlap C Red	Out	11-3
EE	Phase 1 Ped Omit	In	4-1	Overlap D Yellow	Out	11-5
FF	Pedestrian Recycle (Ring 1)	In	6-5	Overlap C Green	Out	11-1
GG	Max II Selection (Ring 1)	In	6-6	Overlap B Green	Out	10-4
HH	I/O Mode Bit C	In	8-8	Overlap C Yellow	Out	11-2

TITLE:
NEMA INTERFACE I/O PORT CONNECTORS A & B

NO SCALE

TEES, NOV 19, 1999

10-5-7

	CONNECTOR C			CONNECTOR D		
PIN	FUNCTION	I/O	PORT-BIT	FUNCTION	I/O	PORT-BIT
A	Coded Status Bit A (Ring 2)	Out	12-4	Detector 9	In	10-1
B	Coded Status Bit B (Ring 2)	Out	12-5	Detector 10	In	10-2
C	Phase 8 Don't Walk	Out	4-8	Detector 11	In	10-3
D	Phase 8 Red	Out	1-8	Detector 12	In	10-4
E	Phase 7 Yellow	Out	2-7	Detector 13	In	10-5
F	Phase 7 Red	Out	1-7	Detector 14	In	10-6
G	Phase 6 Red	Out	1-6	Detector 15	In	10-7
H	Phase 5 Red	Out	1-5	Detector 16	In	10-8
J	Phase 5 Yellow	Out	2-5	Detector 17	In	11-1
K	Phase 5 Ped Clear	Out	5-5	Detector 18	In	11-2
L	Phase 5 Don't Walk	Out	4-5	Detector 19	In	11-3
M	Phase 5 Next	Out	8-5	Detector 20	In	11-4
N	Phase 5 On	Out	9-5	Detector 21	In	11-5
P	Phase 5 Vehicle Detector	In	1-5	Detector 22	In	11-6
R	Phase 5 Pedestrian Detector	In	2-5	Detector 23	In	11-7
S	Phase 6 Vehicle Detector	In	1-6	Detector 24	In	11-8
T	Phase 6 Pedestrian Detector	In	2-6	Clock Update	In	12-1
U	Phase 7 Pedestrian Detector	In	2-7	Hardware Control	In	12-2
V	Phase 7 Vehicle Detector	In	1-7	Cycle Advance	In	12-3
W	Phase 8 Pedestrian Detector	In	2-8	Max 3 Selection	In	12-4
X	Phase 8 Hold	In	3-8	Max 4 Selection	In	12-5
Y	Force Off (Ring 2)	In	7-1	Free	In	12-6
Z	Stop Timing (Ring 2)	In	7-2	Not Assigned	In	12-7
a	Inhibit Max Timing (Ring 2)	In	7-3	Not Assigned	In	12-8
b	Test Input C	In	9-3	Alarm 1	In	13-1
c	Coded Status Bit C (Ring 2)	Out	12-6	Alarm 2	In	13-2
d	Phase 8 Walk	Out	6-8	Alarm 3	In	13-3
e	Phase 8 Yellow	Out	2-8	Alarm 4	In	13-4
f	Phase 7 Green	Out	3-7	Alarm 5	In	13-5
g	Phase 6 Green	Out	3-6	Flash In	In	13-6
h	Phase 6 Yellow	Out	2-6	Conflict Monitor Status	In	13-7
i	Phase 5 Green	Out	3-5	Door Ajar	In	13-8
j	Phase 5 Walk	Out	6-5	Special Function 1	In	14-1
k	Phase 5 Check	Out	7-5	Special Function 2	In	14-2
m	Phase 5 Hold	In	3-5	Special Function 3	In	14-3
n	Phase 5 Omit	In	5-5	Special Function 4	In	14-4
p	Phase 6 Hold	In	3-6	Special Function 5	In	14-5
q	Phase 6 Omit	In	5-6	Special Function 6	In	14-6
r	Phase 7 Omit	In	5-7	Special Function 7	In	14-7
s	Phase 8 Omit	In	5-8	Special Function 8	In	14-8
t	Phase 8 Vehicle Detector	In	1-8	Preempt 1 In	In	15-1
u	Red Rest Mode (Ring 2)	In	7-4	Preempt 2 In	In	15-2
v	Omit All Red (Ring 2)	In	7-7	Preempt 3 In	In	15-3
w	Phase 8 Ped Clear	Out	5-8	Preempt 4 In	In	15-4
x	Phase 8 Green	Out	3-8	Preempt 5 In	In	15-5
y	Phase 7 Don't Walk	Out	4-7	Preempt 6 In	In	15-6
z	Phase 6 Don't Walk	Out	4-6	Alarm 1 Out	Out	12-7
AA	Phase 6 Ped Clear	Out	5-6	Alarm 2 Out	Out	12-8
BB	Phase 6 Check	Out	7-6	Special Function 1 Out	Out	13-1
CC	Phase 6 On	Out	9-6	Special Function 2 Out	Out	13-2
DD	Phase 6 Next	Out	8-6	Special Function 3 Out	Out	13-3
EE	Phase 7 Hold	In	3-7	Special Function 4 Out	Out	13-4
FF	Phase 8 Check	Out	7-8	Special Function 5 Out	Out	13-5
GG	Phase 8 On	Out	9-8	Special Function 6 Out	Out	13-6
HH	Phase 8 Next	Out	8-8	Special Function 7 Out	Out	13-7
JJ	Phase 7 Walk	Out	6-7	Special Function 8 Out	Out	13-8
KK	Phase 7 Ped Clear	Out	5-7	Not Assigned	---	---
LL	Phase 6 Walk	Out	6-6	Detector Reset	Out	11-8
MM	Phase 7 Check	Out	7-7	Not Assigned	---	---
NN	Phase 7 On	Out	9-7	+24 VDC	---	---
PP	Phase 7 Next	Out	8-7	2070N DC Gnd	---	---

TITLE:
NEMA INTERFACE I/O PORT CONNECTORS C & D

NO SCALE

TEES, NOV 19, 1999

10-5-8

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD FCU
3	RXD FCU
4	RTS FCU
5	CTS FCU
6	NA
7	2070-8 DC GND
8	DCD FCU
9	2070-8 DC GND
10	485 TX Data+
11	485 TX Data-
12	485 TX Clock+
13	485 TX Clock-
14	2070-8 DC GND
15	485 RX Data+
16	485 RX Data-
17	2070-8 DC GND
18	485 RX Clock+
19	485 RX Clock-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD 1
3	RXD 1
4	RTS 1
5	CTS 1
6	NA
7	DC GND #1
8	DCD 1
9	AUDIO IN 1
10	AUDIO IN 1
11	AUDIO OUT 1
12	AUDIO OUT 1
13	NA
14	EQ GND
15	TXD 2
16	RXD 2
17	RTS 2
18	CTS 2
19	NA
20	DC GND #1
21	DCD 2
22	AUDIO IN 2
23	AUDIO IN 2
24	AUDIO OUT 2
25	AUDIO OUT 2

TITLE: 2070-8 NEMA MODULE EX1 & EX2 CONNECTOR PINOUTS

NO SCALE

TEES, NOV 19, 1999

10-5-9